88980200 B

CONTROL DATA
CORPORATION

CONTROL DATA®
DA101/DA401 DIGITAL INPUT UNIT

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE MANUAL

88980200

CONTROL DATA
CORPORATION

CONTROL DATA®
DA101/DA401 DIGITAL INPUT UNIT

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
PARTS DATA

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
A	Manual released. Obsoletes and replaces Publication No. 39909502, per ECO DS 13402.
(5/75)	
B	Manual revised per ECO DS 13544; updates logic diagrams.
(5/75)	
Publication No. 88980200	

Address comments concerning this manual to:

Control Data Corporation
Publications and Graphics Division
4455 Eastgate Mall
La Jolla, California 92037
or use Comment Sheet in the back of this manual.

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

MANUAL REVISION	FCO OR ECO	EQUIPMENTS					
		DA101-A	DA101-B	DA104			
A	DS013402	A01, A02	A01, A02	A01, A02			
B	DSD13544	—	—	—			

LIST OF EFFECTIVE PAGES

New features, as well as changes, deletions, and additions to information in this manual are indicated by bars in the margins or by a dot near the page number if the entire page is affected. A bar by the page number indicates pagination rather than content has changed.

Page	Revision	SFC†
Cover	—	
Title Page	—	
Revision Record	B	
iii	B	
iv	B	
v	A	
vii	A	
viii	A	
ix	A	
1.1	A	
1.2	A	
1.3	A	
1.4	A	
2.1	A	
2.2	A	
2.3	A	
3.1	A	
3.2	A	
3.3	A	
3.4	A	
3.5	A	
3.6	A	
3.7	A	
4.1	A	
4.2	A	
4.3	A	
4.4	A	
4.5	A	
4.6	A	
5.1	A	
5.2	A	
5.3	A	
5.4	A	
5.5	A	
5.6	A	
5.7	A	
5.9	A	
5.11	B	
5.12	B	
5.13	B	
5.14	B	
5.15	B	
5.16	B	
5.17	A	
5.18	A	

Page	Revision	SFC†
6.1	A	
6.2	A	
7.1	A	
7.3	B	
7.4	B	
7.5	B	
7.6	B	
7.7	B	
7.8	B	
Comment Sheet	B	
Envelope	B	
Back Cover	B	

†Software Feature Change

PREFACE

This manual describes the DA101/DA401 Digital Input Unit (DIU), which is designed for use in the Real Time Input/Output Module (IOM) product line. The DIU is used in conjunction with the EL101-A Computer Interface Unit/EL102-A Computer Interface Expander.

The following Control Data publications will be useful in installing and maintaining the DIU:

Description	Publication Number
Real Time IOM Product Line Index	88980000
EL101-A Computer Interface Unit/EL102-A Computer Interface Expander Manual	88980100
Input/Output Specification Manual	60165800
1700 Computer Reference Manual	60153100
SMM17 Version 3.0 Reference Manual, Test No. 90	60182000
Electromagnetic Compatibility Design Guide Handbook	CDC-STD-1.30.20

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF TABLES

Section One

GENERAL DESCRIPTION

1.1 GENERAL

This manual describes the Digital Input Unit (DIU) card which plugs into the Computer Interface Unit or the Computer Interface Expander. This manual is to be used in conjunction with the Computer Interface Unit/Computer Interface Expander Manual. The DIU may also be used with any other compatible real-time computer interface unit.

The DIU enables a control computer to sample data produced by external devices having outputs consisting of logic level changes or contact closures. Typical applications of the unit include process monitoring, process control, medical computer and manufacturing test.

The unit contains signal conditioning to accommodate the following in sets of 16 inputs (mutually exclusive):

- Digital logic inputs of 0 and +5 volts (typical), either polarity logical true (within the set); or
- Relay logic inputs consisting of form A, B, or C contact closure, as illustrated in Figures 5.2 and 5.3.

The unit has two modes of operation, asynchronous and synchronous, selectable by jumper on the card. Asynchronous mode allows the control computer to read the state of the digital inputs at any time. Synchronous mode enables the digital input operations to be synchronized with signals from an external device. This latter mode prevents the computer from acquiring ambiguous data which could occur if the inputs were sampled while changing.

1.2 PERFORMANCE/CHARACTERISTICS

1.2.1 PERFORMANCE

Requirements are:

• Number of inputs	16 bits, one word.
• Input source	a. Logic level, 0 and +5 volts, either polarity logical true (within the set); or b. Contact closure consisting of form A, B, or C (as illustrated in Figures 5.2 and 5.3).
• Input overload protection	+70 vdc maximum.
• Input time constant (Signal conditioning delay)	Logic level, 750 nanoseconds. Contact closure, 5 milliseconds.
• Sync operation	Enables digital input operation to be synchronized with signals from an external device.
• Interrupt flag	Occurs when using request sync input from external device.
• Addressing capability	Unit may be connected into any unit location of the Computer Interface Unit (CIU) or Computer Interface Expander (CIE).

- Programming considerations — Data output, function output or status input results in internal reject. Sync mode will generate external reject when data input is attempted without request to input data from external device.
- Configuration — See Table 1.1 and Paragraph 1.3.

1.2.2 RELIABILITY

Requirements are:

- Mean time between failures (MTBF) - Estimated 75,000 hours
- Fail safe features - Inputs contain overload protection and will operate up to +70 vdc maximum. Damage may occur with inputs above +70 vdc.

Table 1.1. DIU Assembly Configurations

EQUIP. NO.	SIGNAL LEVELS (TYPICAL)	
	DATA INPUTS	SYNC INPUTS
DA101-A	Logic level: True = 0 ±0.4 vdc at 1.6 milliamperes False = +2.4 to 5.25 vdc	Logic level, 0v or +5v, true polarity selectable by jumper
DA101-B	Logic level: True = +2.4 to 5.25 vdc False = 0 ±0.4 vdc at 1.6 milliamperes	Logic level, 0v or +5v, true polarity selectable by jumper
DA401-A	N/O contact, input enabled on closure to ground. See Figure 5.2(A).	Form C contact closure See Figure 5.3
DA401-B	N/C contact connected to ground, input enabled upon contact opening. See Figure 5.2(B).	Form C contact closure See Figure 5.3

1.2.3 MAINTAINABILITY

Maintainability provisions are:

- Mean time to repair (MTTR) - Estimated 0.5 hours.
- Preventive maintenance - See Section Six
- Interchangeability - The DIU is a one-card device and may be interchanged with another identical version.
- Diagnostics available - SMM17 Diagnostic, Test 90 of the SMM17 Reference Manual may be used when the DIU is controlled by a CDC 1700/1770 computer. Section 10 of the test exercises reply, reject and sync operation. Section 11 performs a closed loop data test when a digital output unit (DOU) is connected to the DIU.
- Special test equipment required - A digital output unit (Part No. 39842500) is required to perform closed loop data testing with SMM17 Diagnostic, Test 90, Section 11. Refer to the SMM17 Reference Manual.

1.2.4 ELECTROMAGNETIC INTERFERENCE

The DIU is designed in accordance with the Electromagnetic Compatibility Design Guide Handbook.

1.3 EQUIPMENT CONFIGURATION

The DIU is a one-card device that can be inserted into any station address location in the CIU or the CIE. Paragraph 3.3 specifies the cabling required for connecting external input signals to the DIU.

Section Two

OPERATION AND PROGRAMMING

2.1 CONTROLS AND OPERATING PROCEDURE

No controls provided.

2.2 JUMPERS AND OTHER EQUIPMENT CHANGES

2.2.1 MODE JUMPER

A jumper is provided to select asynchronous (ASYNC) or synchronous (SYNC) mode operation. In the ASYNC mode the unit is always ready for input operations. In SYNC mode, the digital inputs are synchronized with signals from an external device. This prevents acquiring ambiguous data which could occur if the inputs were sampled while changing.

2.2.2 NUT-AND-BOLT JUMPERS

Two jumpers are provided for selecting the input polarity on the request and reset signals from an external device. The H position represents a true input for signals going from 0 vdc to +5 vdc.

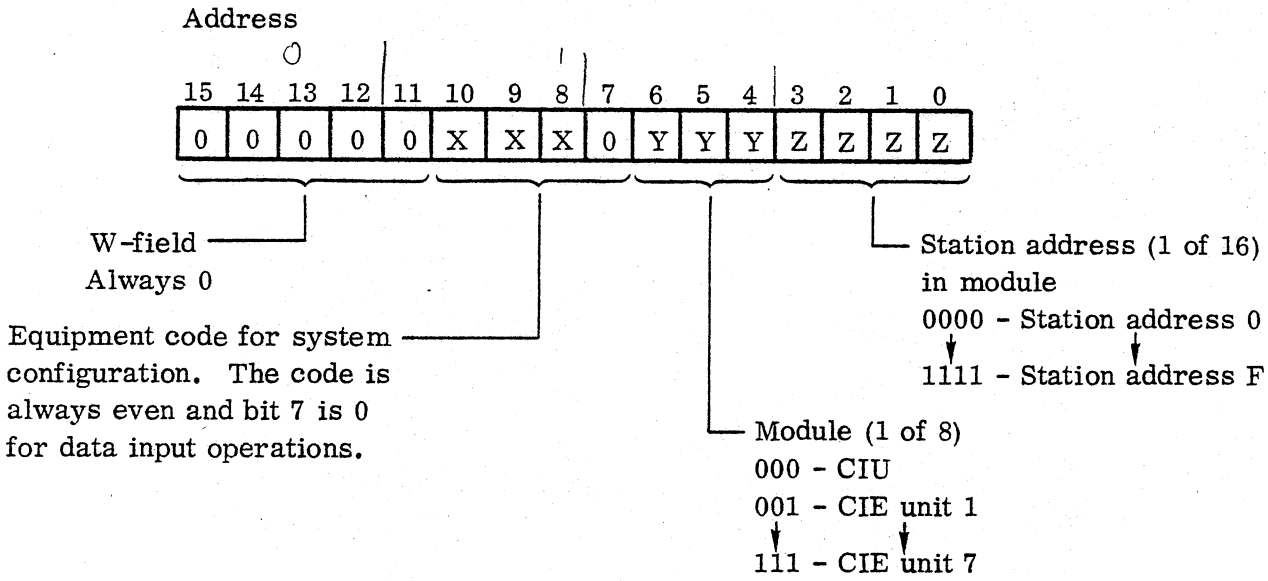
Position L represents a true input for signals going from +5 vdc to 0 vdc. See Figure 5.3 for configuration of form C contact synchronizing signals.

One jumper is provided to select the output polarity of the complete signal to an external device. Position H provides a true output of +5 vdc. Position L provides a true output signal of 0 vdc (ground).

2.3 PROGRAMMING INFORMATION

2.3.1 DATA INPUT

The DIU responds to data input (computer read) operations only. The computer address must specify the station address location of the DIU in a CIU or a CIE. The following CIU/CIE format is used:



Example 1: A computer read from address $0607 will transfer data from a DIU located in station address 7 of a CIU on a system using equipment code C.

Example 2: A computer read from address $042B will transfer data from a DIU located in station address B of CIE module 2 on a system using equipment code 8.

Station addresses for the CIU and CIE may be found in Table 2.1 of the CIU/CIE Manual.

The DIU does not respond to data output (computer write) operations, nor to function output or status input (address bit 7 = 1) operations.

2.3.2 REJECTS

Internal rejects will occur if a data output, function output, or status input operation is attempted on a DIU.

An external reject will occur when the DIU is in SYNC mode and a data input is attempted when the unit is not ready. This is because the unit has not received a sync request from an external device prior to the input operation.

2.3.3 INTERRUPT FLAG

The flag is generated upon receipt of the request signal from an external device. The interrupt flag remains active until a read operation transfers the data and resets the flag.

2.3.4 MASTER CLEAR

A computer console master clear will set the interrupt flag signal and resets and inhibits the complete signal to the external device.

2.3.5 PROGRAMMING CONSIDERATIONS

The DIU does not respond to data output, function output, or status input operations.

Data input operations are always performed using the even equipment code number jumpered on the CIU control.

Section Three

INSTALLATION AND CHECKOUT

3.1 INSTALLATION REQUIREMENTS

The DIU is a one card device 7-3/4 by 9 inches in size. It can be inserted into any station address location in the CIU, in a CIE, or any other compatible real time computer interface unit. Signals from an external device are connected to the DIU by installing a cable on the rear of the CIU or CIE module in the respective station address location.

3.2 POWER REQUIREMENTS

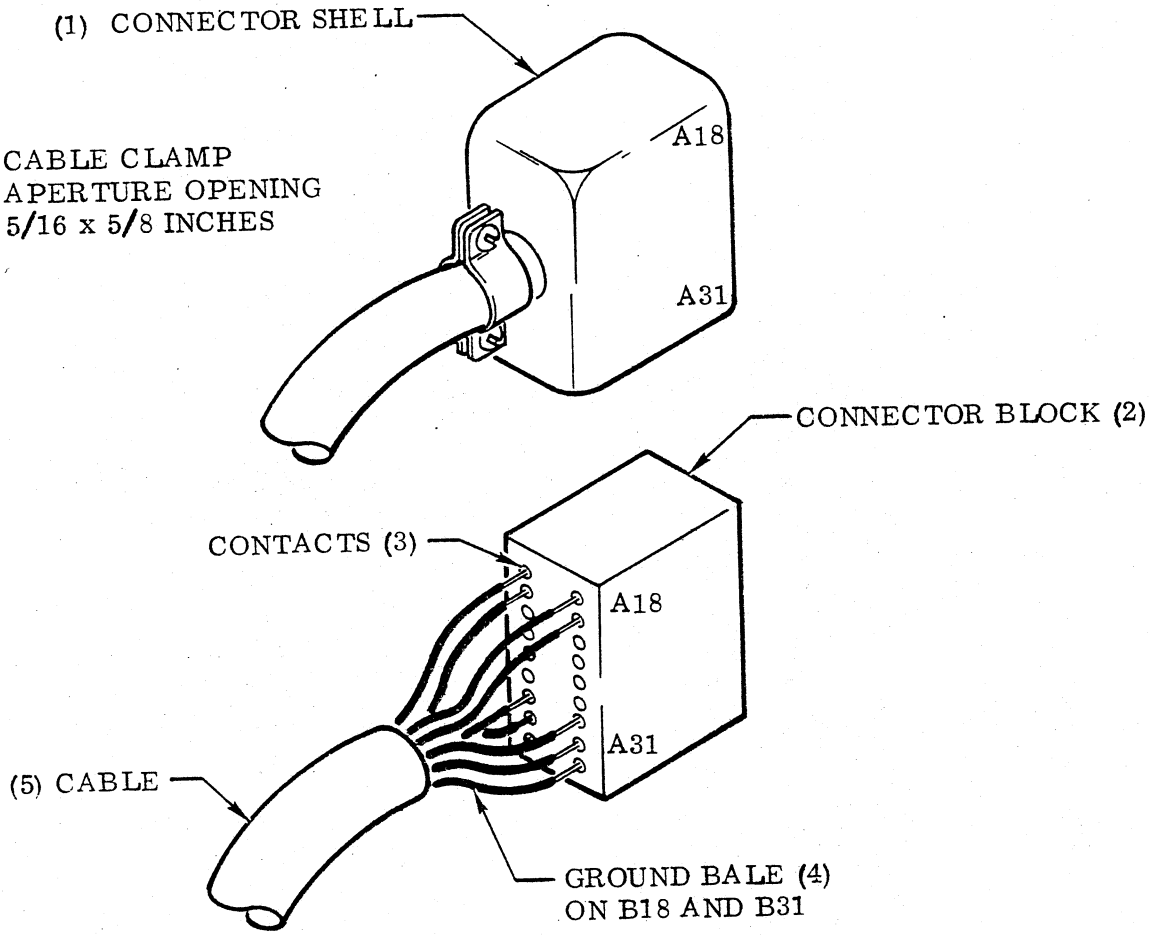
Logic power of +5 vdc is supplied by the CIU or CIE module. The current required by the DIU is 370 milliamperes. Input power for the CIU/CIE power supplies is 115 vac, 50/60 Hz. Power conversion transformer, rack option 10299-22, is required in the system when input power is 220/240 vac, 50 Hz.

3.3 CABLING AND CONNECTORS

External signals are connected to the DIU by installing a customer furnished cable assembly on the rear of the CIU or CIE module at the respective station address location. The connector shell, block, and contacts are supplied with each DIU. These are:

- Connector shell - CDC Part No. 39498600
- Connector Block - CDC Part No. 94261810
- Contacts - CDC Part No. 94245600

A Berg Electronics, Inc., crimp tool No. HT-66 is required for connecting the contacts to the customer furnished cable. Figure 3.1 illustrates a recommended assembly for the input cable.



ITEM	DESCRIPTION	CDC PART NO.	QUANTITY
1	Connector shell (28 pin)	39498600	1
2	Connector block	94261810	1
3	Contacts	94245600	21
4	Ground wire bale, solid 24AWG	(Furnished by customer)	As required
5	Cable, 19 twisted pair, 24AWG	(Furnished by customer)	As required

Figure 3.1. Input Cable Connector Assembly

3.4 INTERFACE CHARACTERISTICS

3.4.1 DATA/CONTROL BUS INTERFACE

The Data/Control Bus between the DOU and the CIU/CIE module is described the CIU/CIE Manual.

3.4.2 EXTERNAL I/O INTERFACE

The signal and pin assignments for interfacing an external device are listed in Table 3.1.

3.4.2.1 Data Signal Levels

Requirements are:

- DA101-A (logic level)

  True = 0 ±0.4 vdc at 1.6 milliamperes
  False = +2.4 to 5.25 vdc

- DA101-B (logic level)

  True = +2.4 to 5.25 vdc
  False = 0 ±0.4 vdc at 1.6 milliamperes

- DA401-A (contacts) - Normally open contact; input enabled upon closure to ground, as illustrated in Figure 5.2(A).

- DA401-B (contacts) - Normally closed contact, connected to ground; input enabled upon contact opening as illustrated in Figure 5.2(B).

Table 3.1. DIU External Interface

PIN NO.	SIGNAL	DESCRIPTION
A18	–	
B18	GND	Ground
A19	INB00	Input data bit 00
B19	INB01	01
A20	INB02	02
B20	INB03	03
A21	INB04	04
B21	INB05	05
A22	INB06	06
B22	INB07	07
A23	INB08	08
B23	INB09	09
A24	INB10	10
B24	INB11	11
A25	INB12	12
B25	INB13	13
A26	INB14	14
B26	INB15	Input data bit 15
A27	–	
B27	–	
A28	RESET	Sync reset to DIU
B28	REQST	Sync request to DIU
A29	COMPL	Complete from DIU
B29	–	
A30	–	
B30	–	
A31	–	
B31	GND	Ground

3.4.2.2 Request Input Signal

Characteristics are:

- DA101-A and DA101-B (logic level)

  True = 0 ±0.4 vdc at 1.6 milliamperes

  False = +2.4 to 5.25 vdc

  Duration = 1 microsecond minimum

  Rise and fall times = Less than 100 nanoseconds for minimum duration signal.

- DA401-A and DA401-B (contacts) - The normally open terminal of isolated form C contacts. Reset generated by normally closed terminal (see Figure 5.3).

NOTE

A jumper is provided on the request signal to select the opposite polarities for a true and false.

3.4.2.3 Reset Input Signal

Characteristics are:

- DA101-A and DA101-B (logic level)

  True = 0 ±0.4 vdc at 1.6 milliamperes

  False = +2.4 to 5.25 vdc

  Duration = 1 microsecond minimum

  Rise and fall times = Less than 100 nanoseconds for minimum duration signal.

- DA401-A and DA401-B (contacts) - The normally closed terminal of isolated form C contacts. Request generated by normally open terminal (see Figure 5.3).

NOTE

A jumper is provided on the reset signal to select the opposite polarities for a true and false. The reset signal must be jumpered for a true when not used in SYNC mode.

3.4.2.4 Complete Output Signal

This signal is a logic level output as follows for all versions of the DIU:

- True = 0 ±0.5 vdc at 65 milliamperes
- False = +5 ±0.5 vdc via 470 ohms
- Duration = 1 microsecond minimum; normally true until request is false and reset is true.

NOTE

A jumper is provided on the complete signal to select the opposite polarities for a true and false.

3.5 COOLING REQUIREMENTS

An air flow of 350 cfm is required across the DIU in system applications to assure adequate component life time. Standard air flow is provided when the DIU is inserted in a CIU/CIE system. Refer to the Computer Interface Unit/ Computer Interface Expander Manual.

3.6 ENVIRONMENTAL LIMITATIONS

Refer to the Computer Interface Unit/Computer Interface Expander Manual.

3.7 PREPARATION FOR USE

Verify mode jumper in proper position.

Verify request, reset and complete signal jumpers select proper polarity for system operation in SYNC mode.

Verify reset signal jumpered for true (position H) if not used in system application.

Section Four

THEORY OF OPERATION

4.1 GENERAL

The DIU, when connected in a CIU or CIE, enables a control computer to sample logic level and contact closure data produced by external devices. The DIU contains all the signal conditioning required to interface to external devices, and the control logic for communicating with the CIU/CIE. The DIU is a data input device only and provides no status or function capability.

Figure 5.1 is a simplified block diagram and Table 4.1 defines the signal mnemonics and terms. Figure 5.7 is the logic package for the DIU.

4.2 PRINCIPLE OF OPERATION

Operation of the DIU can be either asynchronous mode or synchronous mode. In the asynchronous mode, control is provided by the computer. In the synchronous mode, control is provided by the external device. The input circuits on the DIU provide signal conditioning for either logic level inputs or contact closure inputs. When a data transfer is performed, the state of all 16 inputs (bits) on the DIU is transferred to the computer.

In the following descriptions, a logical 1 is +2.4 to 5.25 vdc, a logical 0 is 0.4 vdc or less, and the timing tolerances are ±25%.

4.2.1 SIGNAL CONDITIONING

4.2.1.1 Data Input Signals

The DIU provides signal conditioning circuits for logic level inputs or contact closures. The logic level circuits have an input time constant of less than two

microseconds to filter out erroneous noise. The contact closure circuits provide an input time constant of 5 milliseconds to eliminate contact bounce. See Paragraph 3.4.2 for the data signal levels.

4.2.1.2 External Sync Signals

Jumpers are provided for selecting the proper input/output polarities for external synchronizing signals.

- Request - A signal from the external device to the DIU indicating an input data word is ready to be sampled. The circuit responds to a logical 1 as a true input when the jumper is in position H. A logical 0 is a true input when the jumper is in position L.
- Complete - A signal from the DIU to the external device indicating the input word has been sampled and transferred to the computer. The jumper in position H provides a logical 1 for a true output. Position L provides a logical 0 as a true output.
- Reset - A signal from the external device to the DIU resetting the sync logic. (This signal is not normally used for logic level inputs.) The jumper in position H responds to a logical 1 as a true input. Position L responds to a logical 0 as a true input.

NOTE

When no reset input signal is connected to the DIU, the reset jumper must be placed in position H for proper sync operation.

4.2.2 ASYNCHRONOUS MODE OPERATION

Input data is transferred from the external device to the computer upon a read command to the DIU station address. The data transfer sequence is illustrated in Figure 5.4 and occurs as follows:

- The REPLY/REJECT FF is placed in the REPLY state when the DIU is not active.
- The DIU connects to the input operation when the station select signal (TP28) becomes a logical 1 and signal FUSTF remains a logical 1 on the bus.
- Upon receipt of a read signal (TP24 becomes a logical 1), the DIU gates the 16 data inputs and a reply to the computer.
- The input operation is terminated when the read (TP24) and station select (TP28) signals return to a logical 0. The REPLY/REJECT FF remains in the REPLY state since an external reject is never generated in asynchronous mode.

The request and reset inputs are not used in asynchronous mode. A one-microsecond complete signal, denoting an input transfer has been performed, is sent to the external device when the jumper on the reset signal is in the H position.

4.2.3 SYNCHRONOUS MODE OPERATION

4.2.3.1 Sync Reply Sequence

Data transfers in synchronous mode are controlled by the external device. The data transfer reply sequence is illustrated in Figure 5.5 and occurs as follows:

- The external device places the data word on input to the DIU, drops the reset signal (when being used), and sends a request signal.

- The request sets the INT/SYNC FF (TP26 becomes logical 1) and reset (TP29) drops to logical 0.
- The DIU flag (FLXXF) is sent to the CIU/CIE, which in turn generates an interrupt to the computer. A read cycle is then initiated upon receipt of the interrupt.
- The DIU responds to the read when station select (TP28) becomes a logical 1, signal FUSTF remains a logical 1, and read (TP24) becomes logical 1.
- Data is then transferred to the computer and a reply is sent.
- The transfer is terminated when station select (TP28) and read (TP24) return to a logical 0. The REPLY/REJECT FF remains in the REPLY state.
- At the time data is transferred to the computer, a complete signal (TP17) is sent to the external device, and the INT/SYNC FF is cleared (TP26 becomes logical 0).
- The complete signal remains true until the request signal from the external device is false and the reset signal is true (if reset is used).

The reset signal permits the external device to control the reset of the synchronizing logic after an input operation. It is used when synchronizing from relay contacts or logic level signals that do not settle in one microsecond. On contact synchronization, the request and reset signals are generated by opposite sides of the form C contacts.

When the reset signal is not connected to the DIU, the jumper for reset control is placed in the H position. The complete signal to the external device is then present for either:

- Approximately one microsecond when the request signal input is a pulse of one microsecond duration; or

- Remains true until request drops (where the complete signal is used to drop request).

4.2.3.2 Sync Reject Sequence

The DIU is normally not ready for data transfers in sync mode. If the computer initiates a data transfer prior to the DIU receiving a request from the external device, the DIU sends a reject to the computer. The reject sequence is illustrated in Figure 5.6 and occurs as follows:

- No request is received from the external device, therefore the INT/SYNC FF is not set (TP26 logical 0).
- The station select signal (TP28 logical 1) enables REJECT ENABLE one-shot that sets the REPLY/REJECT FF to the REJECT state.
- When the read signal (TP24 logical 1) is received, a reject is sent to the computer. The REJECT state also inhibits sending a complete signal to the external device.
- The reject sequence terminates when read (TP24) and station select (TP28) return to logical 0. The REPLY/REJECT FF is set to the REPLY state, ready for the next transfer operation.

4.2.4 ASYNCHRONOUS MODE WITH INTERRUPT

The DIU can be operated in async mode and uses the request input signal to generate a flag (interrupt) to the computer. The sequence is identical to the sync mode reply sequence, but the computer can initiate and complete a data transfer with or without a request being present. The REJECT ENABLE one-shot that places the REPLY/REJECT FF in the REJECT state is never enabled. The DIU, therefore, always sends a reply to the computer.

4.2.5 MASTER CLEAR

The DIU does not contain a programmable master clear. A computer console master clear will set the INT/SYNC FF. The master clear will also reset the COMPL FF and inhibit sending a complete signal to the external device.

Table 4.1. Glossary of Terms

TERM	DEFINITION
DB00F - DB15F	Data bits 00-15 false (To CIU/CIE Common Bus)
INB00 - INB15	Input data bits 00-15 (from external device).
MCLRF	Master clear false (from bus)
READF	Read false (from bus)
FUSTF	Function/status false (from bus)
SSXXF	Station select false (from bus)
FLXXF	Flag line false (to bus)
RPLYF	Reply false (to bus)
RJCTF	Reject false (to bus)
REQST	Request sync (from external device)
COMPL	Complete (to external device)
RESET	Reset sync (from external device)

Section Five

DIAGRAMS

5.1 GENERAL

This section contains the following diagrams:

Figure No.	Title
5.1	Digital Input Unit Block Diagram
5.2	Contact Closure, Data Inputs
5.3	Form C Contact Closure Synchronizing Signals
5.4	Asynchronous Mode Reply Sequence
5.5	Synchronous Mode Reply Sequence
5.6	Synchronous Mode Reject Sequence
5.7	Digital Input Unit Logic Package

5.2 DIAGRAMS

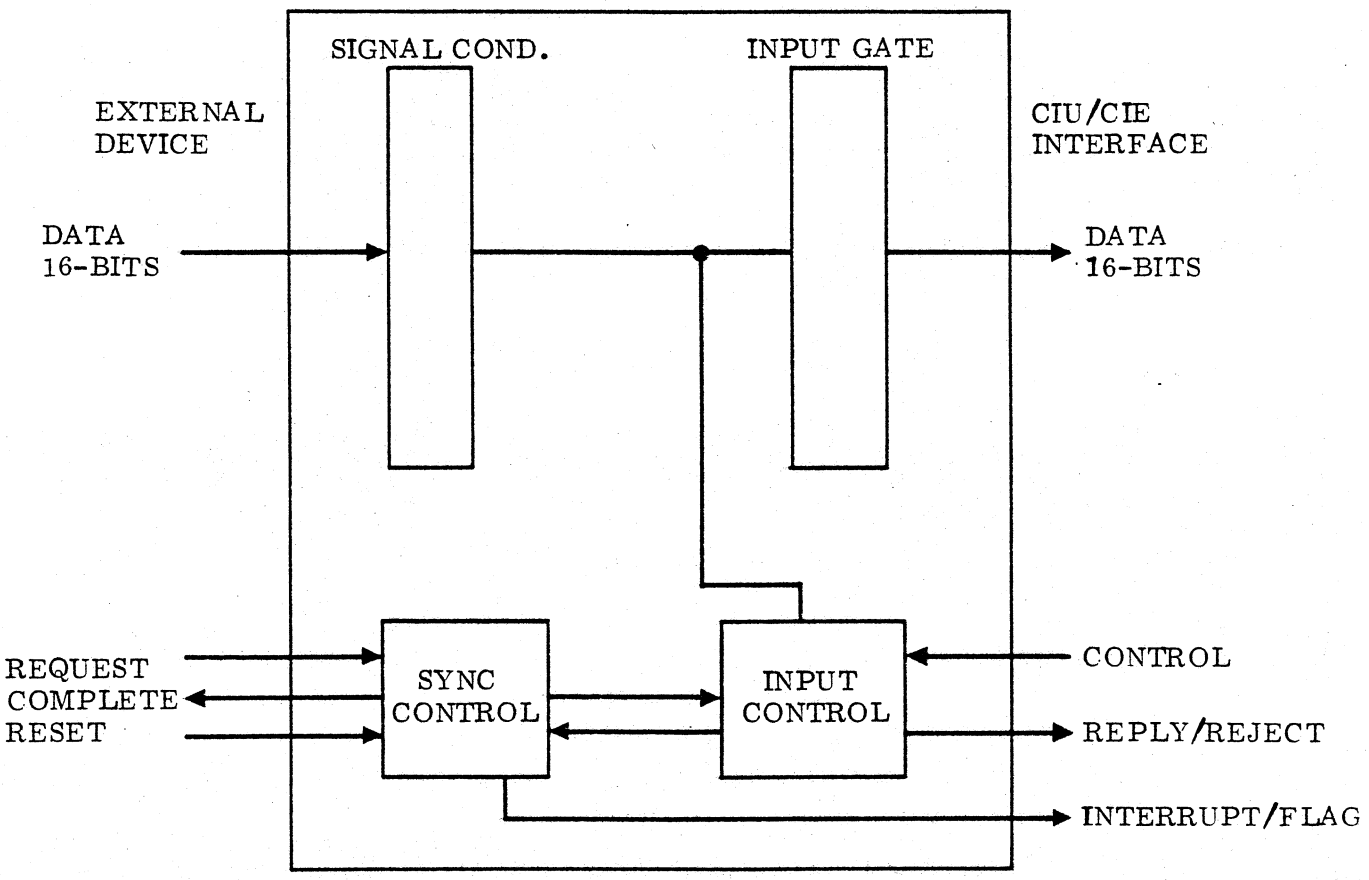
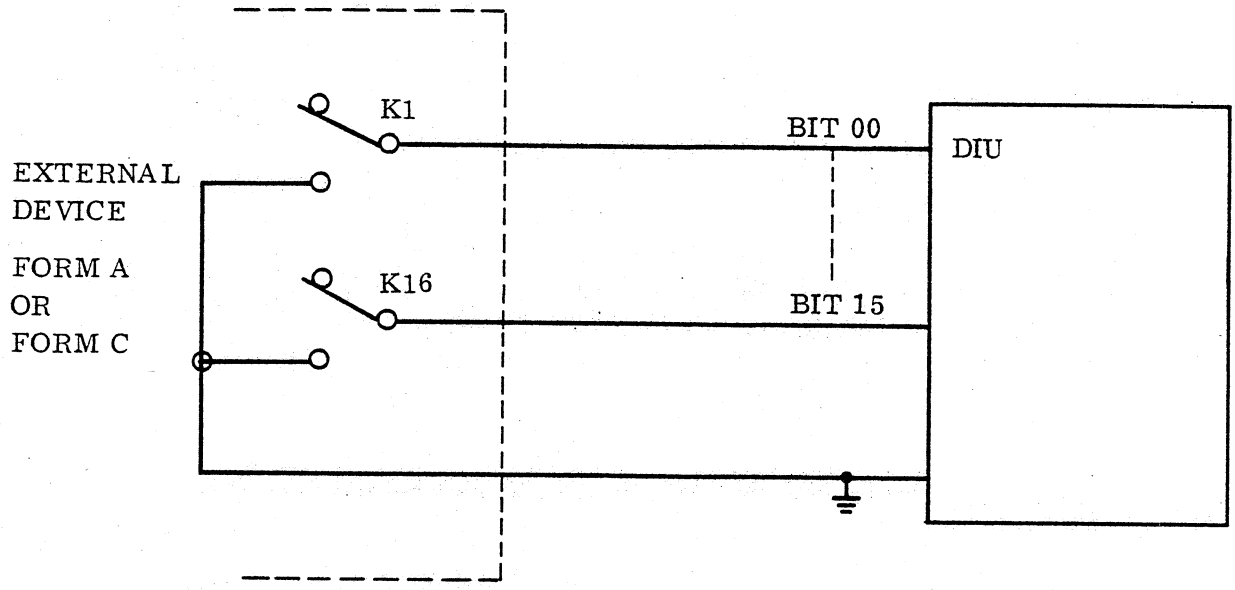
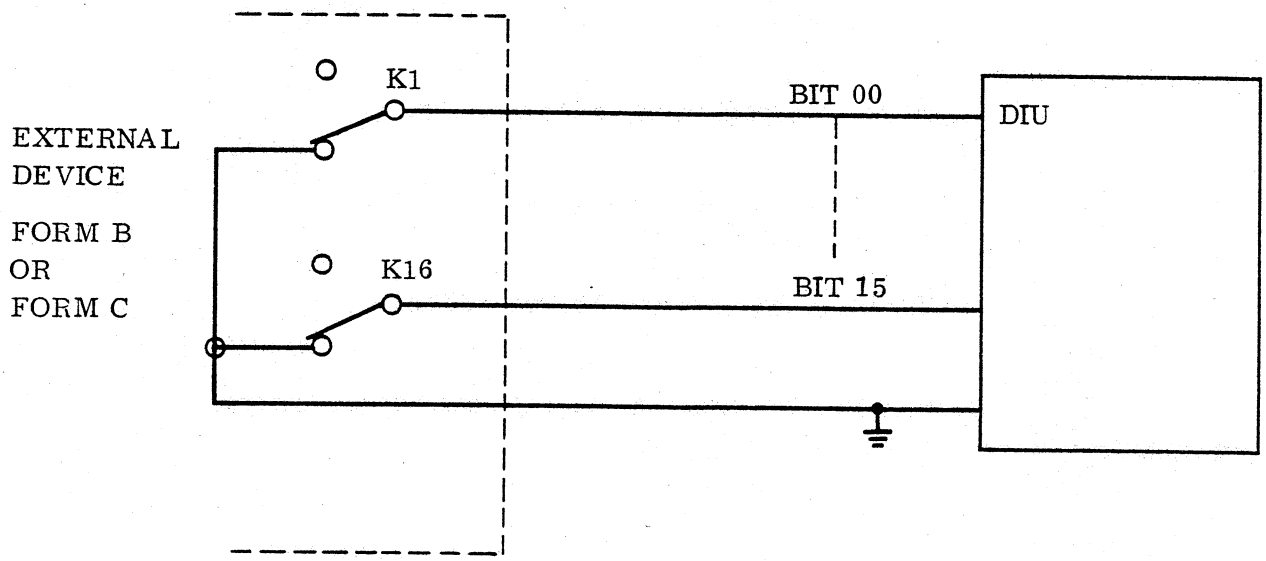


Figure 5.1. Digital Input Unit Block Diagram



(A) NORMALLY OPEN CONTACTS



(B) NORMALLY CLOSED CONTACTS

Figure 5.2. Contact Closure, Data Inputs

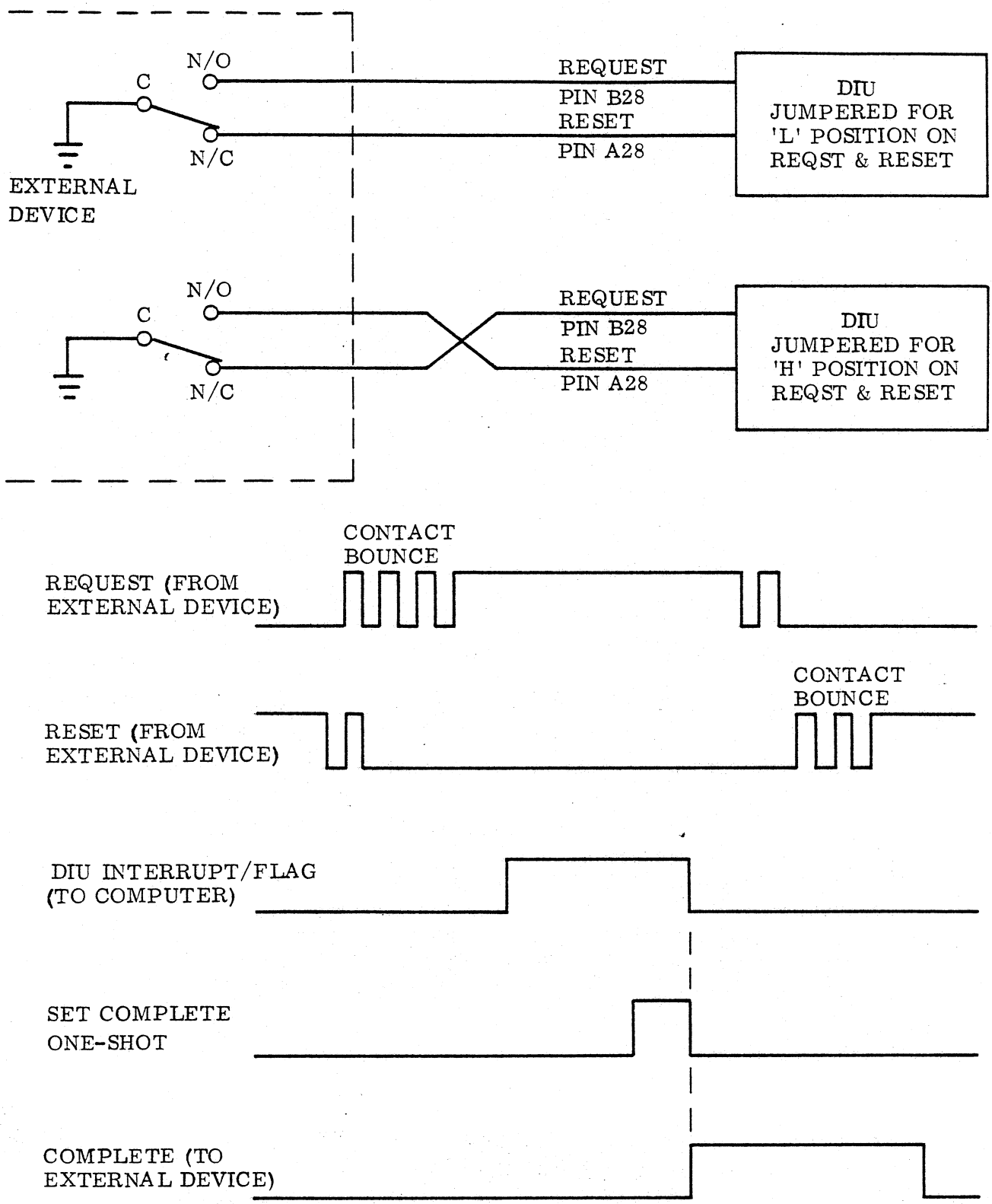


Figure 5.3. Form C Contact Closure Synchronizing Signals

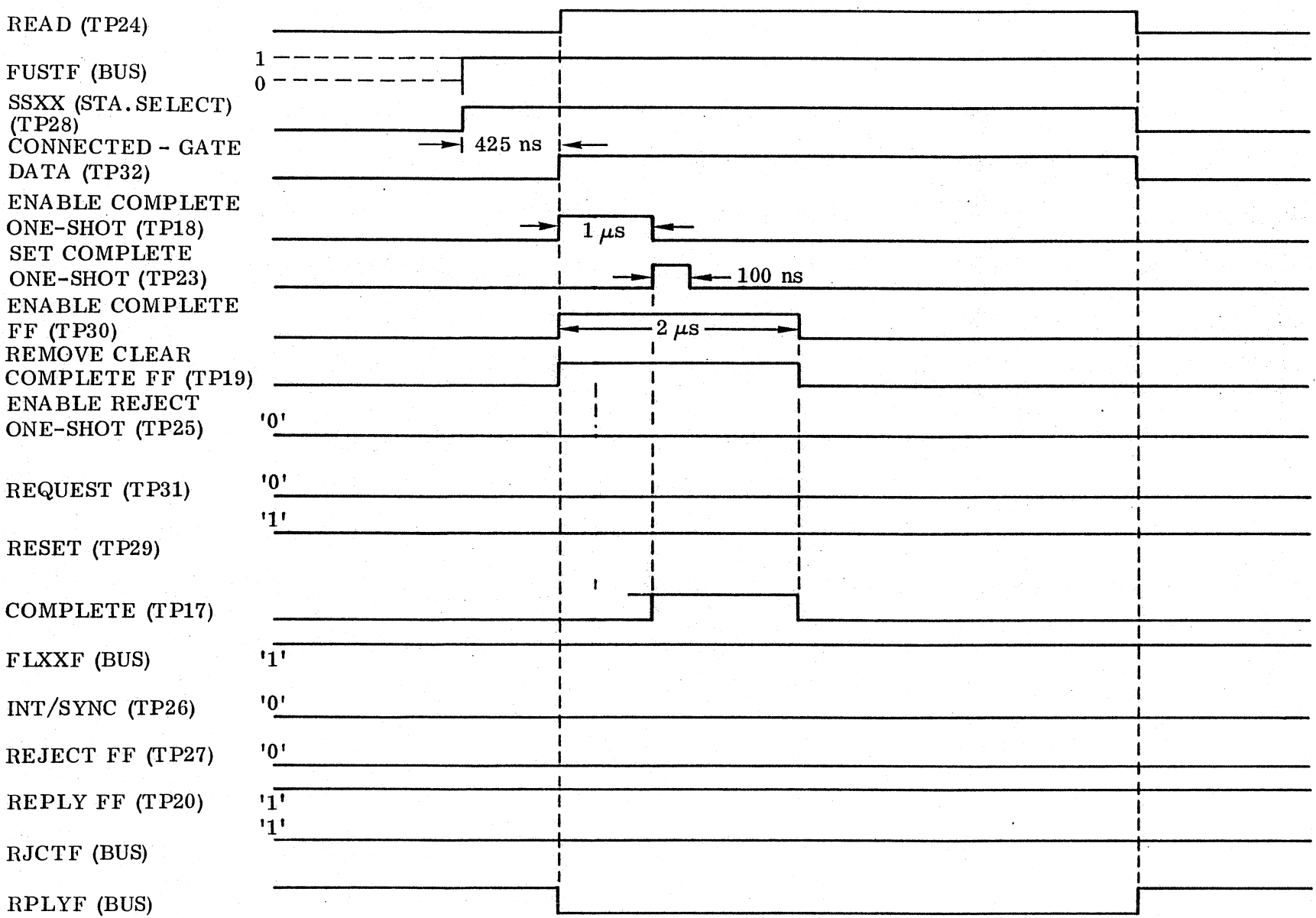


Figure 5.4. DIU Asynchronous Mode Reply Sequence

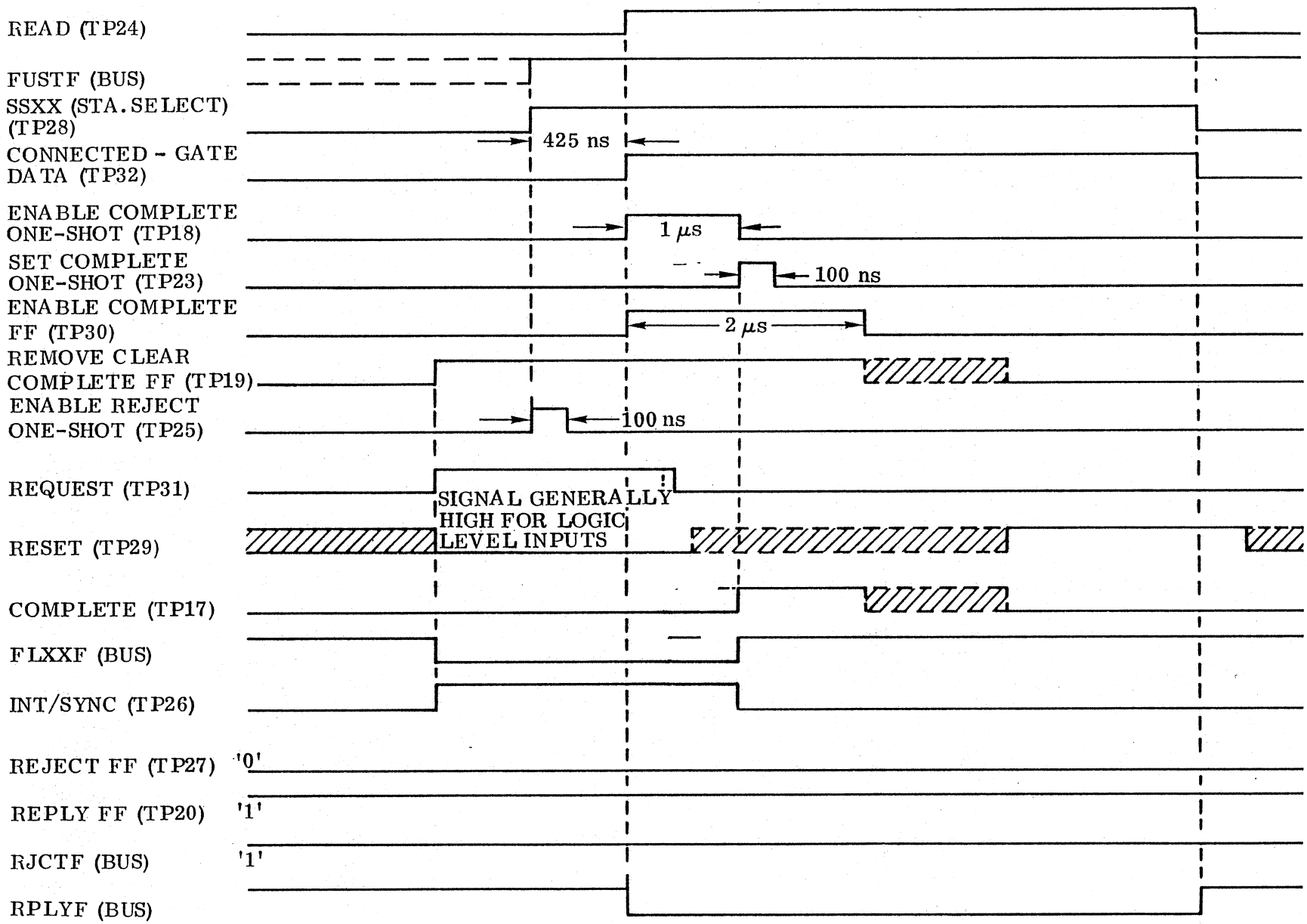


Figure 5.5. DIU Synchronous Mode Reply Sequence

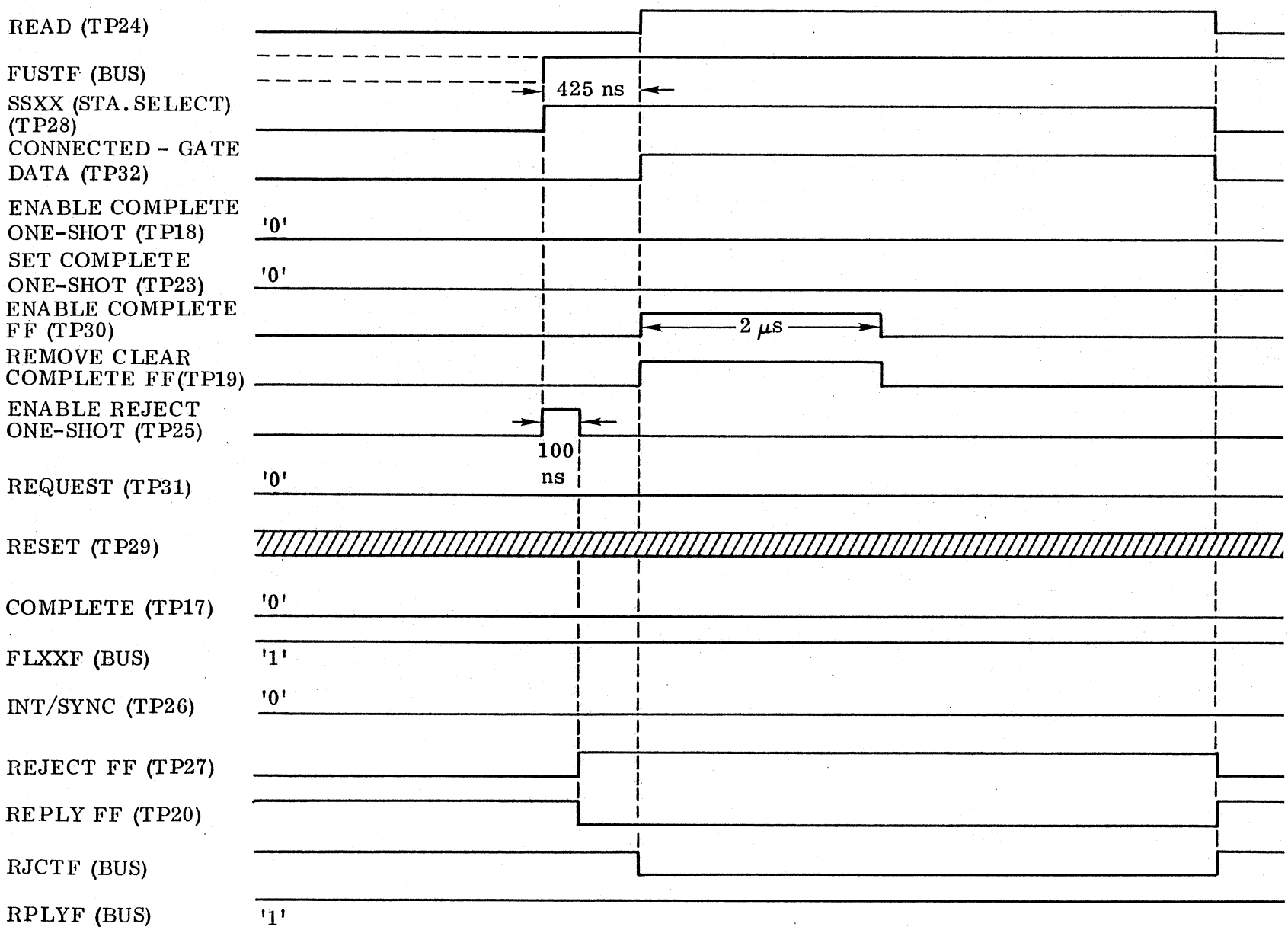
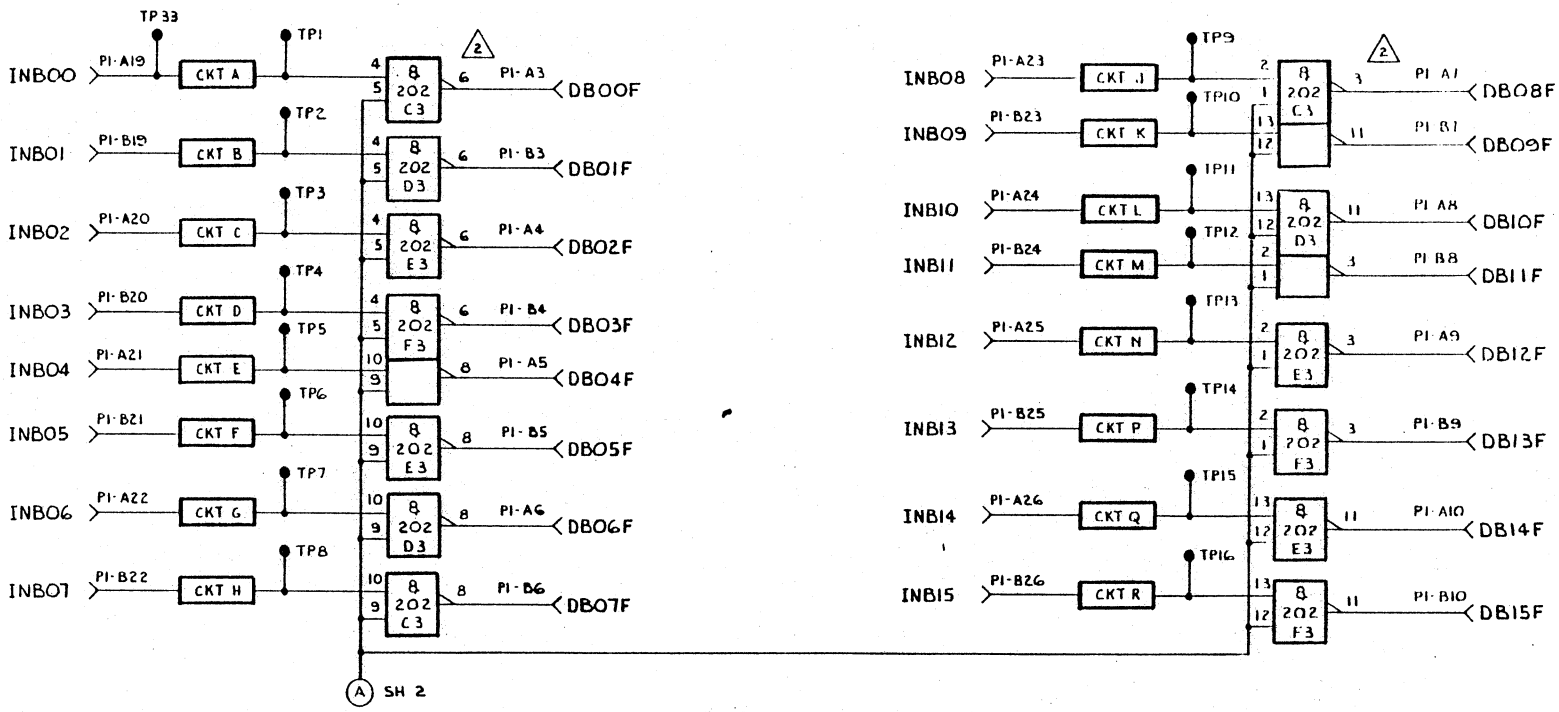
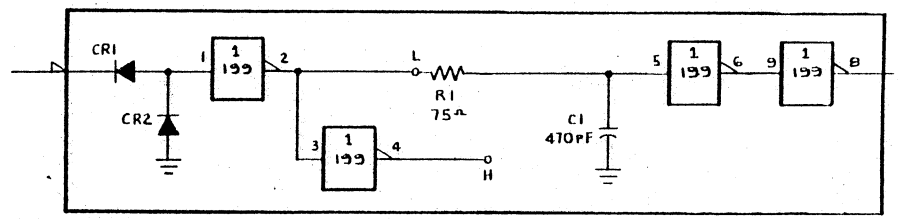


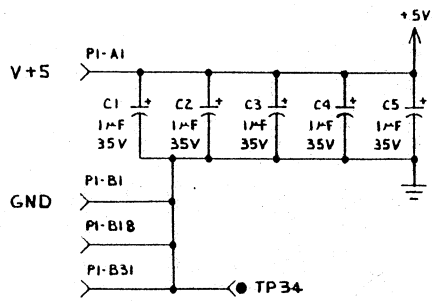
Figure 5.6. DIU Synchronous Mode Reject Sequence

Figure 5.7. Digital Input Unit Logic Package





DISCRETE I C CKT (840)
(TYP A THRU R)



3. FOR KEY TO SYMBOLS SEE DWG 88981500.

2 ALL ELEMENT IDENTIFIERS 202 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39842300 DETACHED LIST

	A	B	C	D	E	F
1		7400	7440	7474	74123	74L04
2		7403	7474	74123	7440	74L04
3			7403	7403	7403	7403
4			CKT A	CKT B	CKT C	CKT D
5		CKT J	CKT H	CKT G	CKT F	CKT E
6		CKT K	CKT L	CKT M	CKT N	CKT P
7			CKT S	CKT T	CKT Q	CKT R

LOGIC TITLE
DIGITAL INPUT UNIT — LL, GND = LOGIC 1

LOGIC DWG NO 39842300 SH 1 OF 2 REV D

PWA NO 39842200 PWB NO 39842100

CONTROL DATA ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif 92037

FIRST USED ON	DA101A	
DR		7 19 72
CHK		7-24-72
ENGR		7-24-72
MFG		7-26-72
APPD		7-26-72
		7-27-72

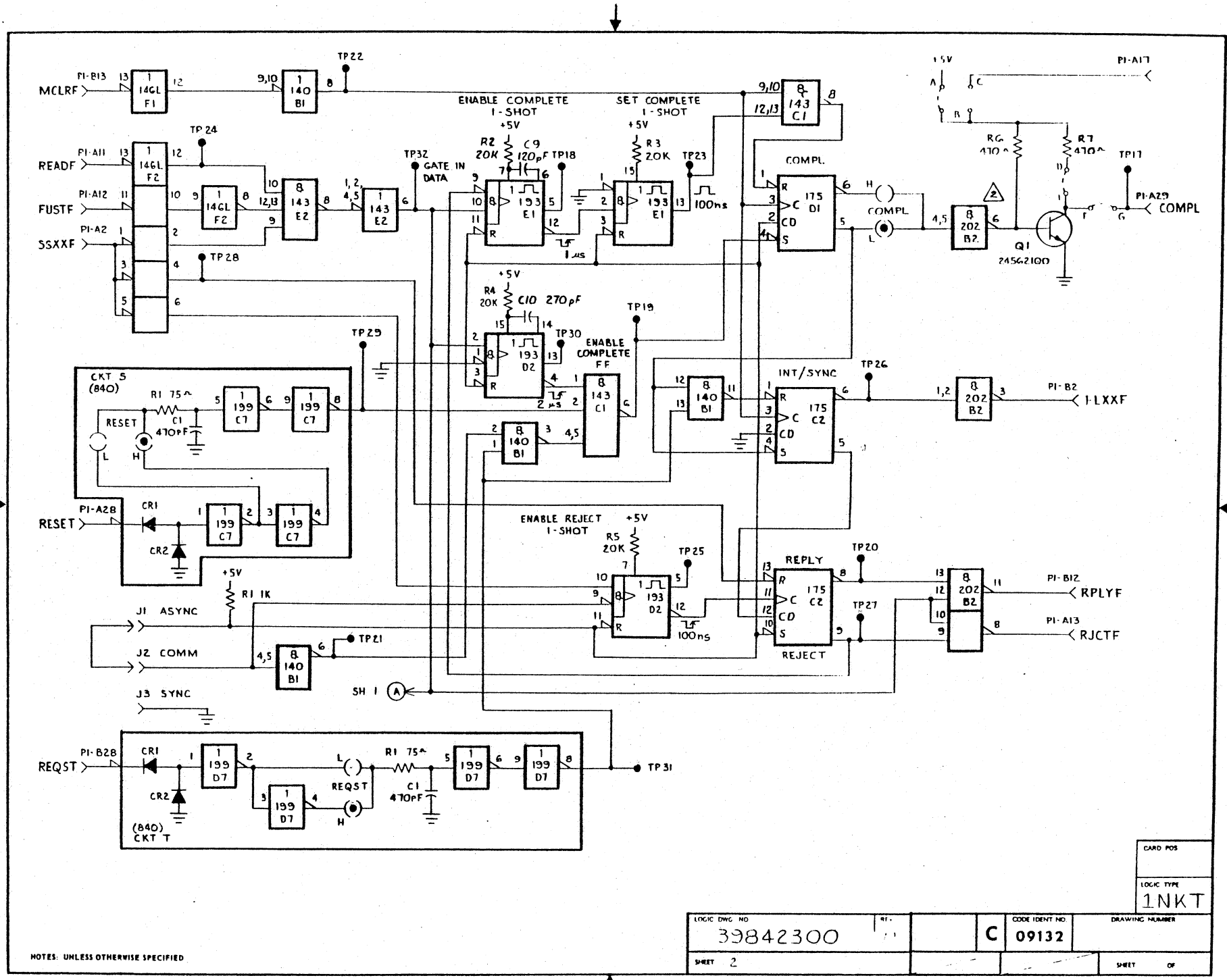
TITLE

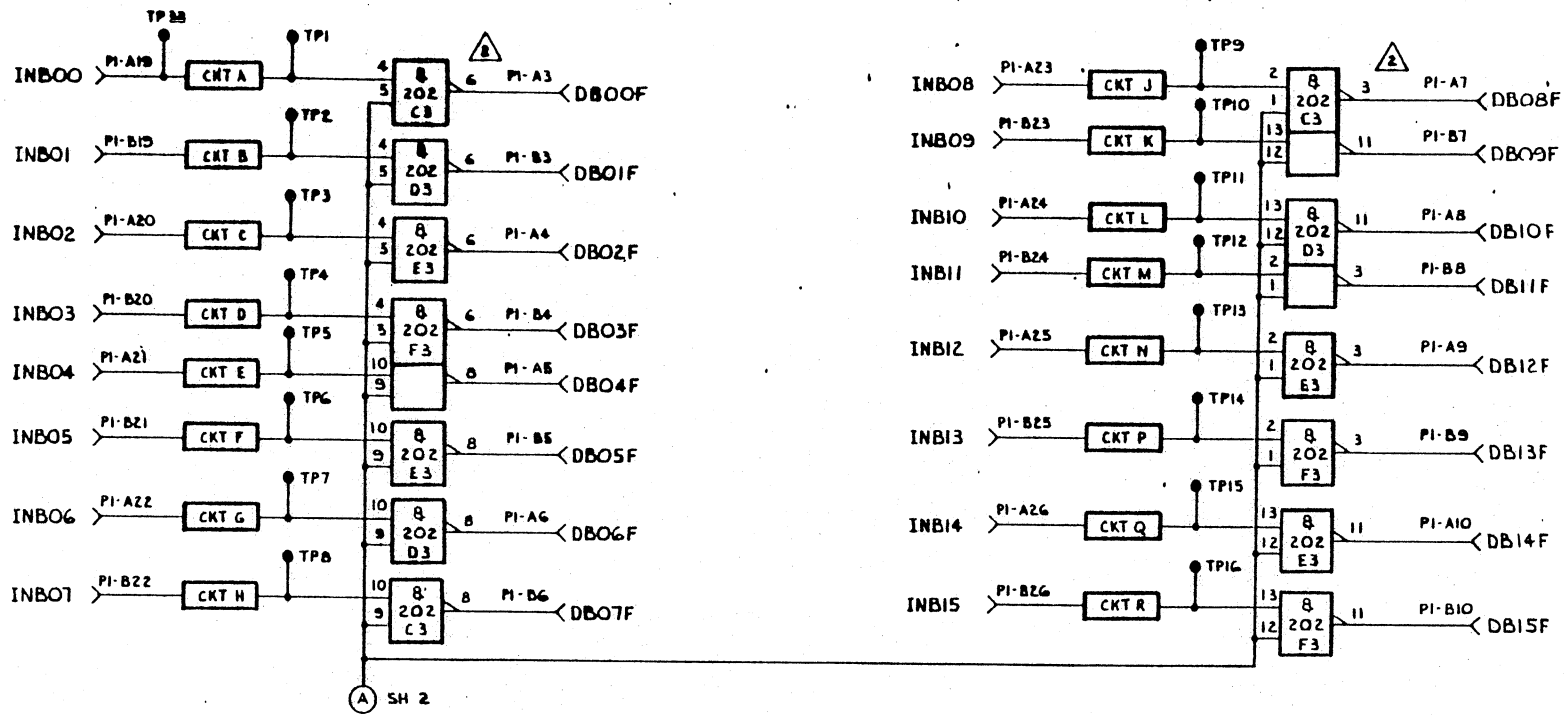
CARD POS

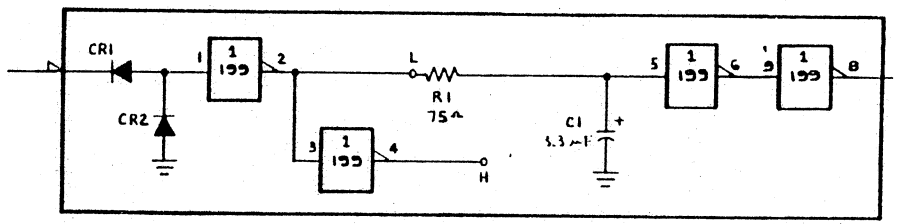
LOGIC TYPE 1NKT

C | CODE IDENT NO 09132 | DRAWING NUMBER

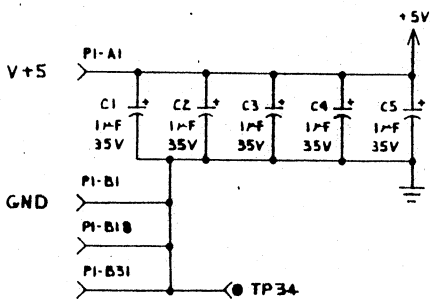
SHEET OF


MCLRF
READF
FUSTF
SSXXF
RESET
REQST
ENABLE COMPLETE 1-SHOT
SET COMPLETE 1-SHOT
GATE IN DATA
ENABLE COMPLETE FF
ENABLE REJECT 1-SHOT
COMPL
INT/SYNC
REPLY
REJECT
J1 ASYNC
J2 COMM
J3 SYNC
RESET
REQST
CKT S (840)
(840) CKT T
PI-A17
PI-A29 COMPL
PI-B2 I-LXXF
PI-B12 RPLYF
PI-A13 RJCTF
Q1 2N5962100
NOTES: UNLESS OTHERWISE SPECIFIED
LOGIC DWG NO 39842300
CODE IDENT NO 09132
DRAWING NUMBER
SHEET 2
CARD POS
LOGIC TYPE 1NKT





DISCRETE & I C CKT (840)
(TYP A THRU R)



2 ALL ELEMENT IDENTIFIERS 202 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

DR 39915100 DETACHED LIST

	A	B	C	D	E	F
1		7400	7440	7474	74123	74L04
2		7403	7474	74123	7440	74L04
3			7403	7403	7403	7403
4			CKT A	CKT B	CKT C	CKT D
5		CKT J	CKT H	CKT G	CKT F	CKT E
6		CKT K	CKT L	CKT M	CKT N	CKT P
7			CKT S	CKT T	CKT Q	CKT R

LOGIC TITLE: DIGITAL INPUT UNIT — CC, GND CONT = LOGIC 1

LOGIC DWG NO: 39915100 SH 1 OF 2 REV C

PWA NO: 39842202 PWB NO: 39842100

CONTROL DATA — ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif 92037

FIRST USED ON	DA401A	
DR	B. Johnson	1-19-72
CHK	G. Gilbert	1-19-72
ENGR	R.W. Ziegler	2-29-72
MFG		
APPD	G. Nixon	7-26-72
	[illegible]	7-27-72

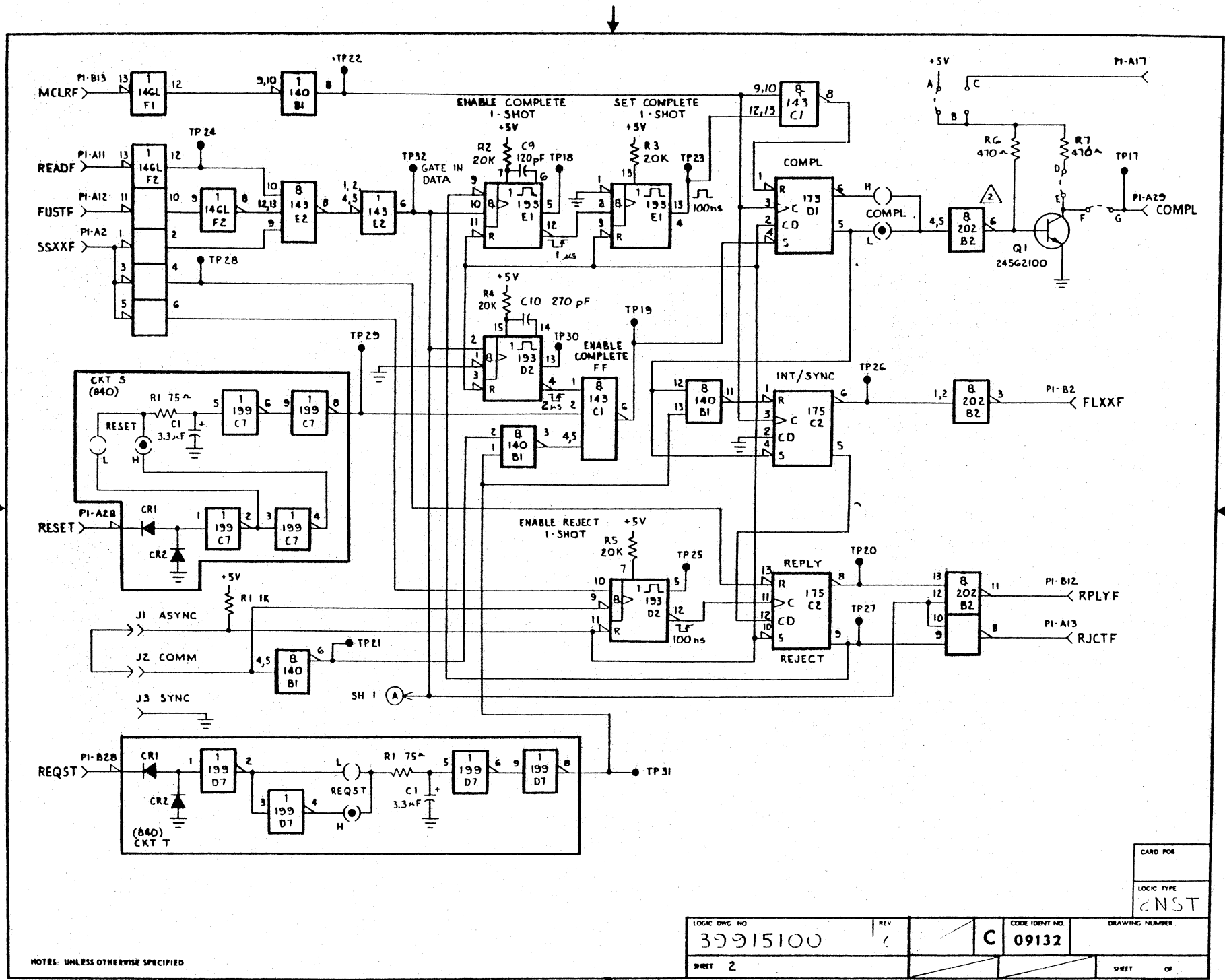
TITLE

CARD POS

LOGIC TYPE 2NST

C | CODE IDENT NO 09132 | DRAWING NUMBER

SHEET OF



NOTES: UNLESS OTHERWISE SPECIFIED

LOGIC DWG NO 39915100	REV		C	CODE IDENT NO 09132	DRAWING NUMBER
SHEET 2					SHEET OF

CARD POS

LOGIC TYPE CNST

Section Six

MAINTENANCE

6.1 PREVENTIVE MAINTENANCE

None required.

6.2 CALIBRATION AND ALIGNMENT

Not required.

6.3 TROUBLESHOOTING

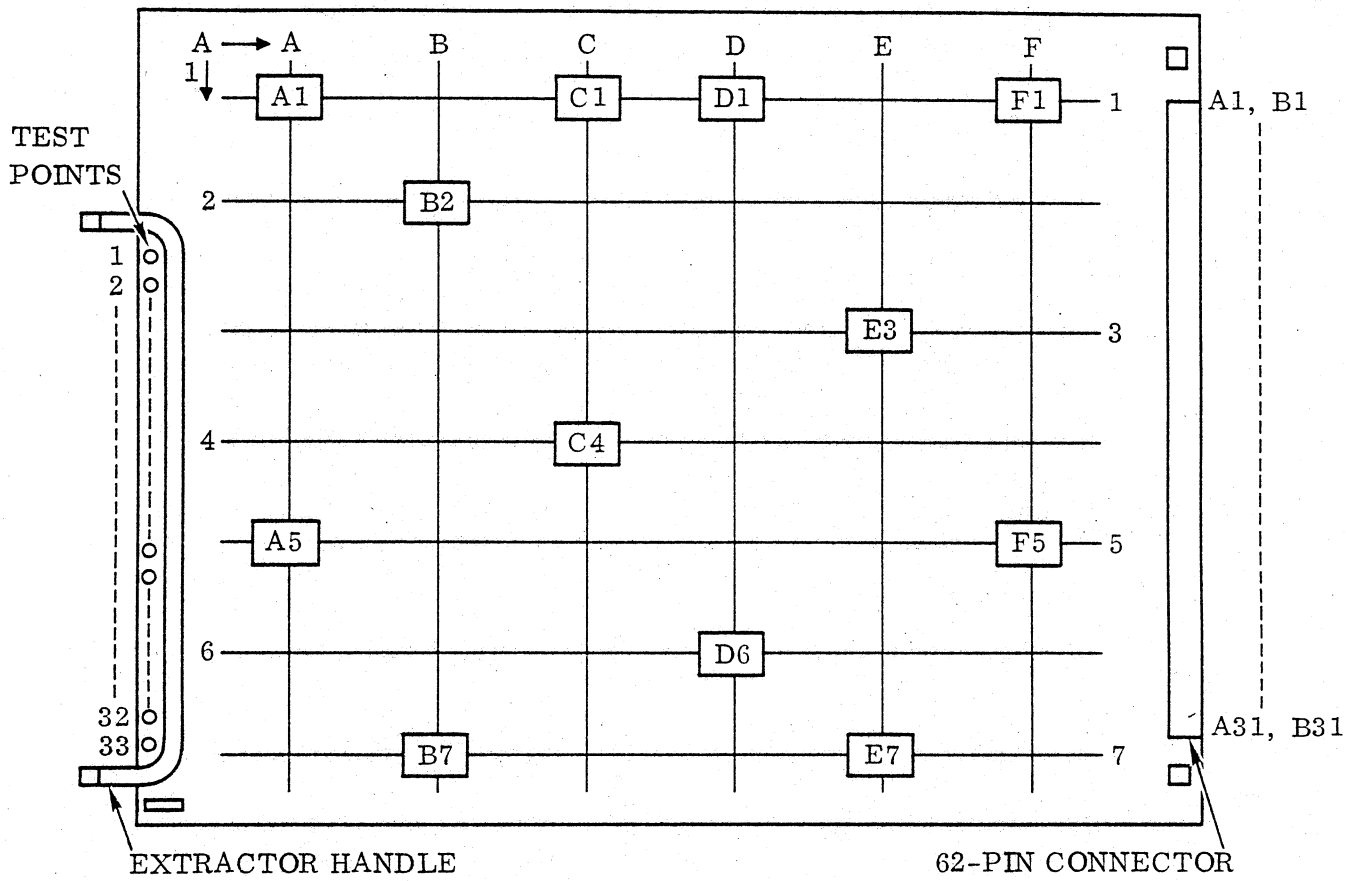
Troubleshooting can be performed on the DIU (when controlled by a 1700/1770 computer) by using Section 10 of Test 90, SMM17 diagnostic. Refer to the SMM17 Reference Manual. Section 11 can be performed when a Digital Output Unit (DOU) is connected to the DIU. Error printouts are provided specifying the instruction performed, expected and actual results, and the condition causing the error.

The DIU can be interchanged with a like version for troubleshooting when the jumpers for mode, request, reset, and complete signals are properly positioned.

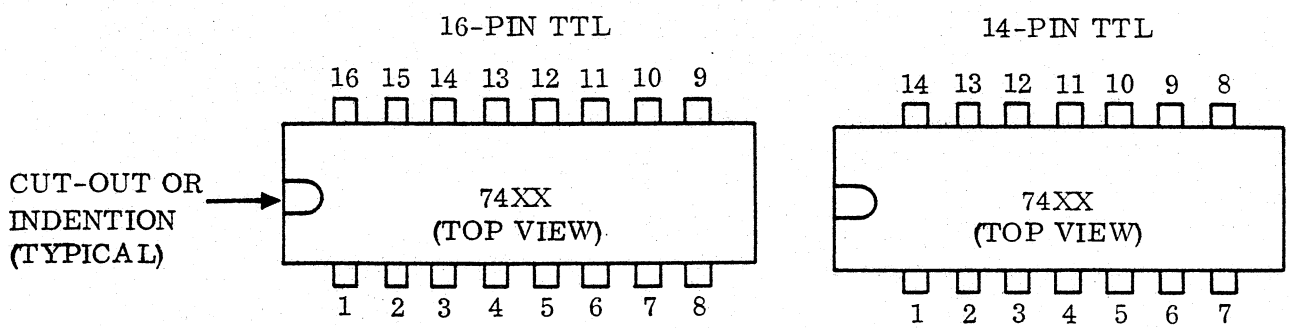
6.4 MAINTENANCE AIDS

Use the following as maintenance aids:

- Card Extender, 9-inch logic type, 2NMT Card No. 39844100.
- Digital Output Unit (DOU), Part No. 39842500.
- Standard pin and chip locations (see Figure 6.1).
- Integrated circuit logic symbols are shown in the Key to Logic Symbols manual, Publication No. 39909515.



PRINTED WIRING BOARD (PWB) COMPONENT SIDE CHIP LOCATION



PIN CONFIGURATION, TOP VIEW

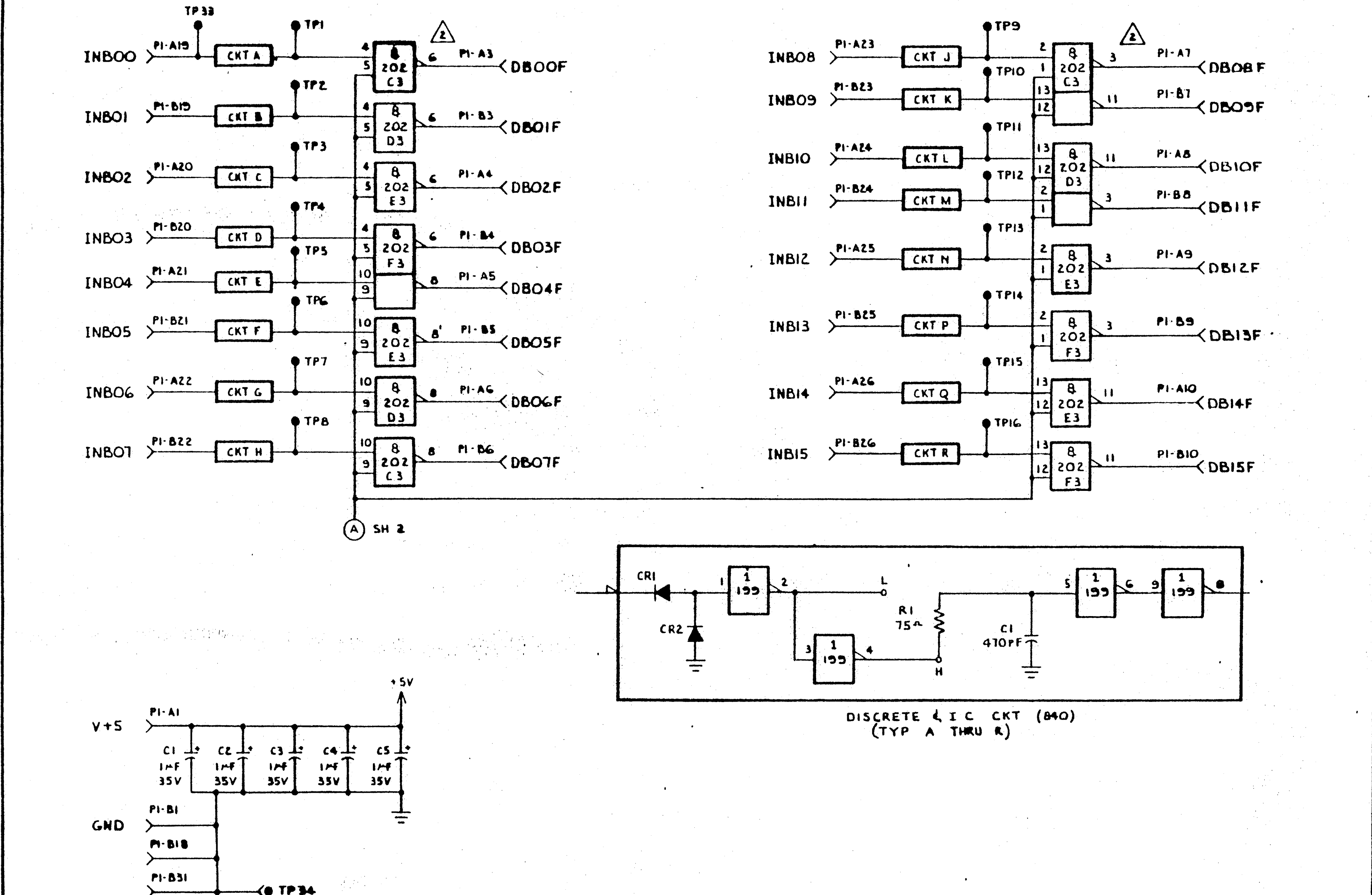
Figure 6.1. Board Component and Pin Location

Section Seven

PARTS DATA

7.1 PARTS DATA

This section contains the printed wiring assembly and parts lists for the digital input unit (DIU).



⚠2 ALL ELEMENT IDENTIFIERS 202 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES: UNLESS OTHERWISE SPECIFIED

39915000 DETACHED LIST

	A	B	C	D	E	F
1		7400	7440	7474	74123	74L04
2		7403	7474	74123	7440	74L04
3			7403	7403	7403	7403
4			CKT A	CKT B	CKT C	CKT D
5		CKT J	CKT H	CKT G	CKT F	CKT E
6		CKT K	CKT L	CKT M	CKT N	CKT P
7			CKT S	CKT T	CKT Q	CKT R

LOGIC TITLE: DIGITAL INPUT UNIT — LL, +5V = LOGIC 1

LOGIC DWG NO: 39915000 SH 1 OF 2 — REV C

PWA NO: 39842201 — PWB NO: 39842100

CONTROL DATA — ANALOG-DIGITAL SYSTEMS DIVISION, La Jolla, Calif 92037

FIRST USED ON: DA101B

DR	[signature]	7-19-72
CHK	[signature]	7-19-72
ENGR	[signature]	7-24-72
MFG	[signature]	7-26-72
APPD	[signature]	7-21-72

TITLE

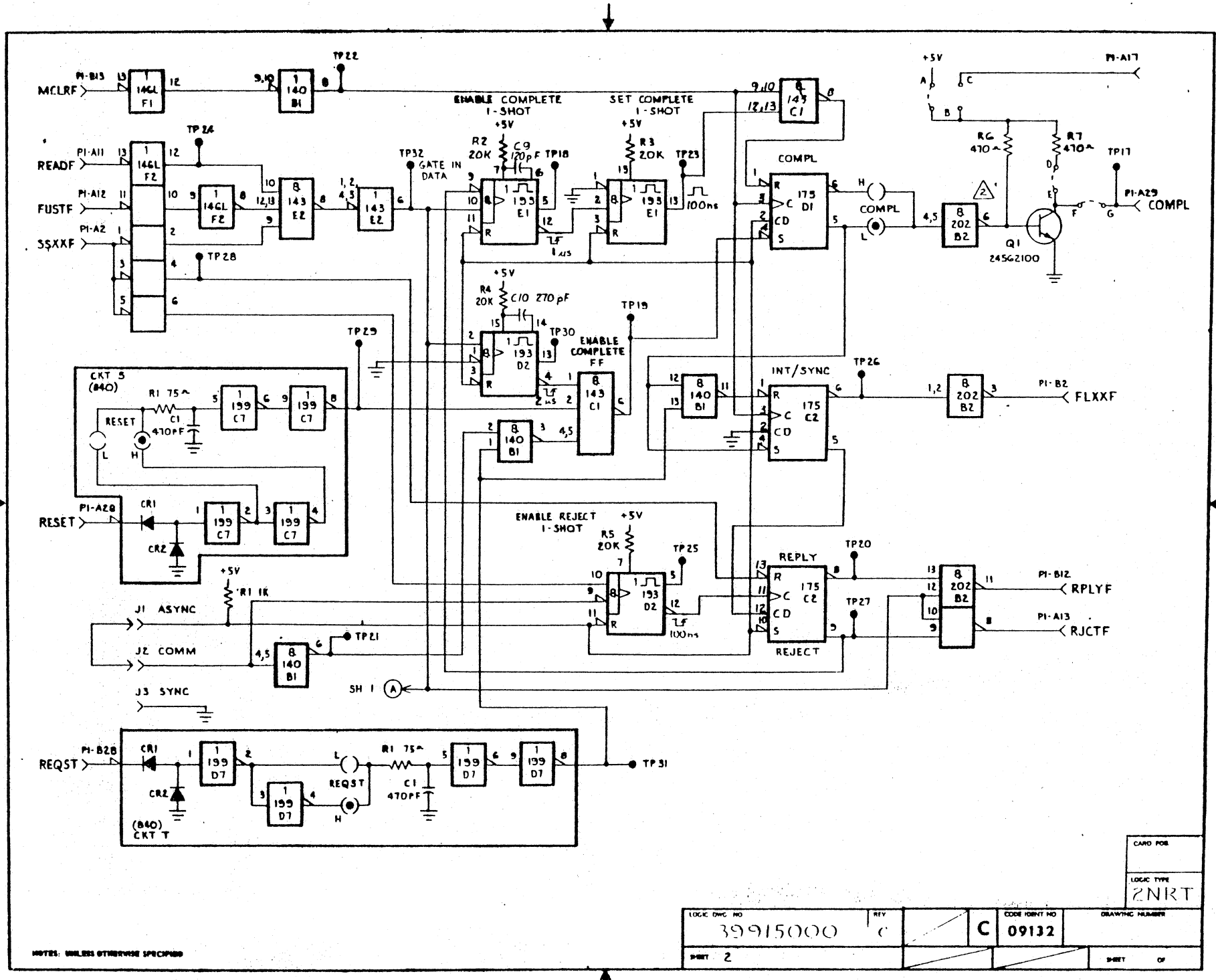
CARD POS

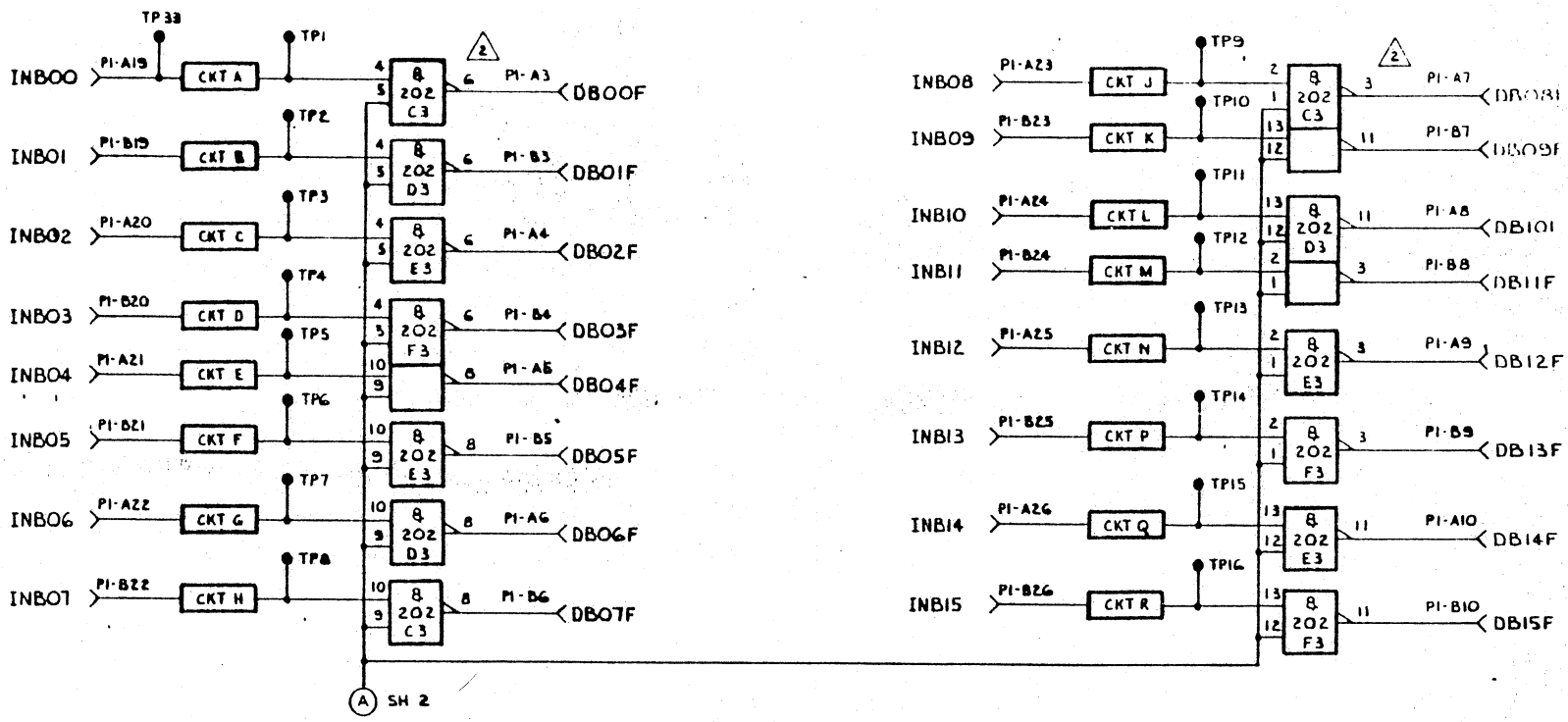
LOGIC TYPE: 2NRT

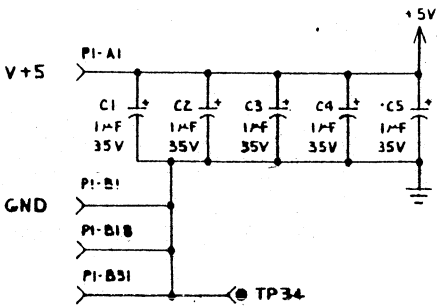
C — CODE IDENT NO: 09132

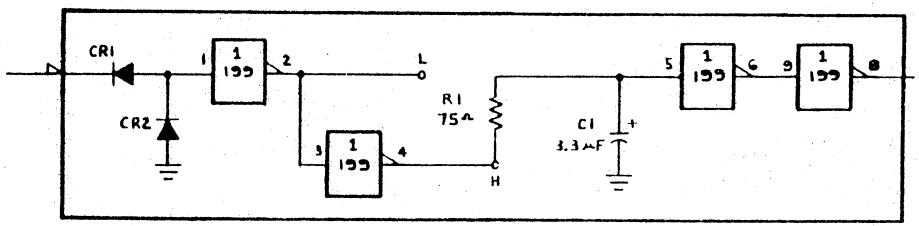
DRAWING NUMBER

SHEET OF


MCLRF
READF
FUSTF
SSXXF
RESET
REQST
ENABLE COMPLETE 1-SHOT
SET COMPLETE 1-SHOT
GATE IN DATA
ENABLE COMPLETE FF
ENABLE REJECT 1-SHOT
COMPL
INT/SYNC
REPLY
REJECT
J1 ASYNC
J2 COMM
J3 SYNC
FLXXF
RPLYF
RJCTF
Q1
2456210O
CKT 5 (840)
(840) CKT T
LOGIC DWG NO 3991500O
REV C
CODE IDENT NO 09132
DRAWING NUMBER
SHEET 2
LOGIC TYPE 2NRT







DISCRETE L I C CKT (840)
(TYP A THRU R)

2 ALL ELEMENT IDENTIFIERS 202 ARE OPEN COLLECTOR.

1. ALL RESISTORS ARE 1/4 W.

NOTES UNLESS OTHERWISE SPECIFIED

DR 39915200 DETACHED LIST

	A	B	C	D	E	F
1		7400	7440	7474	74123	74L04
2		7403	7474	74123	7440	74L04
3			7403	7403	7403	7403
4			CKT A	CKT B	CKT C	CKT D
5		CKT J	CKT H	CKT G	CKT F	CKT E
6		CKT K	CKT L	CKT M	CKT N	CKT P
7			CKT S	CKT T	CKT U	CKT R

LOGIC TITLE: DIGITAL INPUT UNIT — CC, OPEN CONT = LOGIC 1

LOGIC DWG NO: 39915200 SH 1 OF 2 REV B

PWA NO: 39842203 PWB NO: 39842100

CONTROL DATA ANALOG - DIGITAL SYSTEMS DIVISION La Jolla Calif 92037

	FIRST USED ON	
	DA401B	
DR		1-13-72
CHK		1-17-72
ENGR		1-19-72
MFG		
APPD		1-26-72
		1-31-72

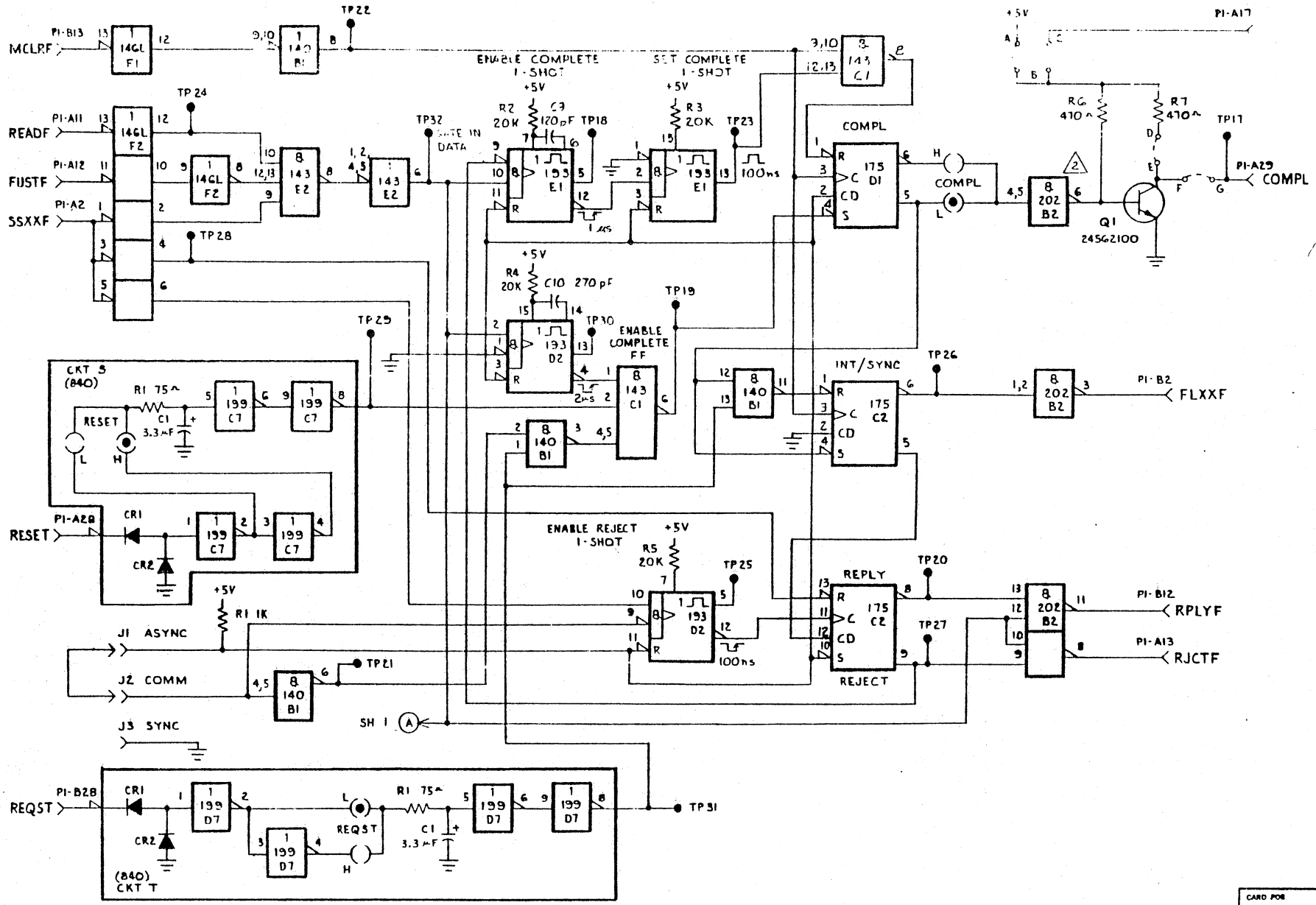
TITLE

CARD POS

LOGIC TYPE 2N11

C | CODE IDENT NO 09132 | DRAWING NUMBER

SHEET OF



NOTES UNLESS OTHERWISE SPECIFIED

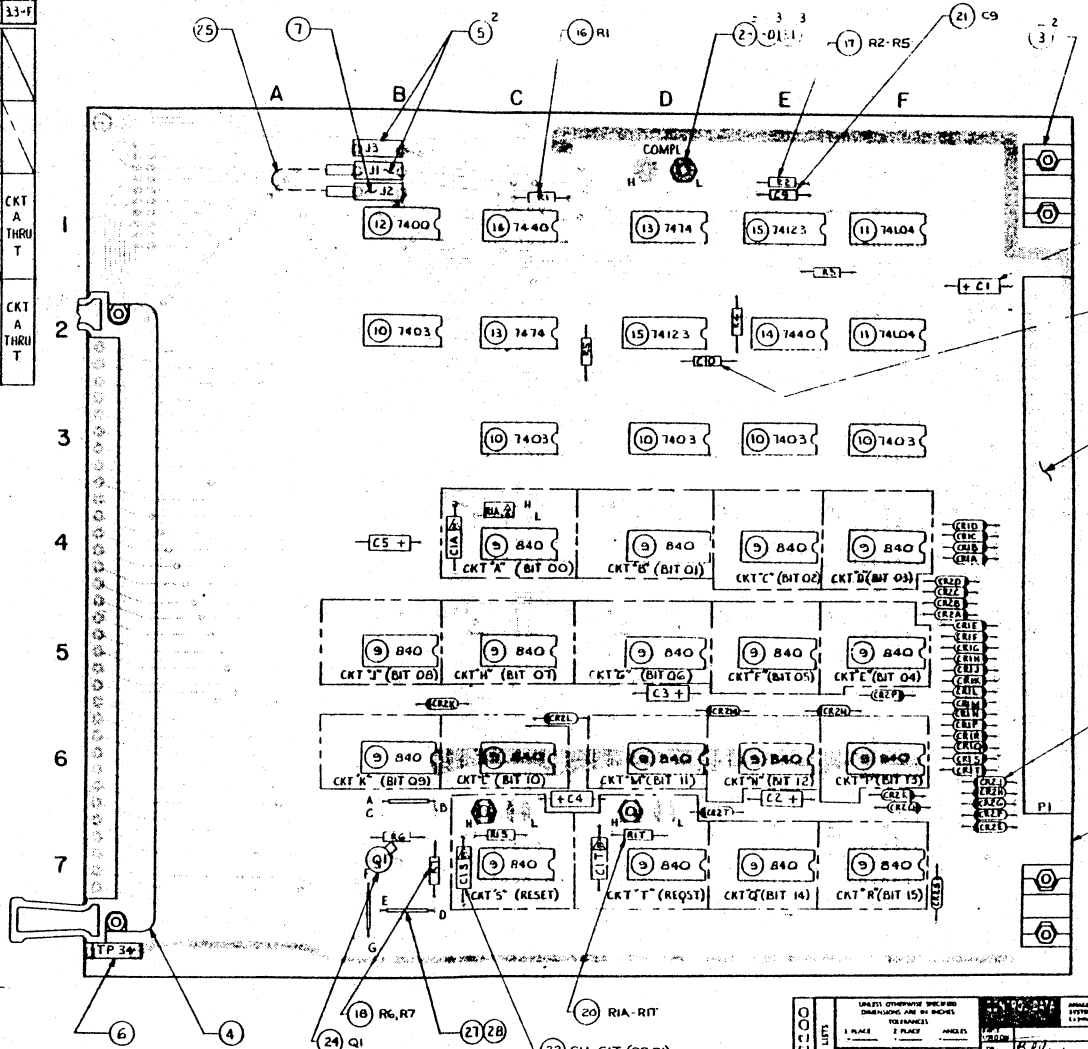
LOGIC DWG. NO 39915200	REV B		C	CODE IDENT NO 09132	DRAWING NUMBER
SHEET 2					SHEET OF

CARD POS

LOGIC TYPE 2NTT

PART NO.	EQUIP NO.	LOGIC TYPE	LOGIC NO.	FUNCTION (16 INPUTS)	COMPONENTS REQ'D RES LOC L	RES LOC H	CAP 470pf	CAP 33-F
39842200	DA101A	1NKT	39942300	L.L.; +5V, GND; GND YIELDS LOGIC 1	CKT A THRU R		CKT A THRU T	
39842201	DA101B	2NRT	39915000	L.L.; GND, +5V; +5V YIELDS LOGIC 1		CKT A THRU R	CKT A THRU T	
39842202	DA401A	2NST	39915100	C.C.; N/O CONT, GND; GND CONT YIELDS LOGIC 1	CKT A THRU R			CKT A THRU T
39842203	DA401B	2NTT	39915200	C.C.; GND, N/O CONT; OPEN CONT YIELDS LOGIC 1		CKT A THRU R		CKT A THRU T

REVISION RECORD					
REV.	ECO	DESCRIPTION	DFT	DATE	CHK
A			BD	12-23-71	
B	13111	RELOCATED C6, ADDED C10	TC	2-18-72	
C	13214	AUTOMATED P/L	DM	2-21-72	
D	13228	ADDED P/N CALLOUTS	WJ	4-17-72	
E	13298	P/L CHG. ONLY	WJ	7-11-72	
F	13544	SEE ECO	WJ	11-15-72	



⚠ SEE TAB.

1. TO BE ASSEMBLED TO CDC ENGR. SPEC. 39721800.

NOTES: UNLESS OTHERWISE SPECIFIED

DO NOT SCALE DRAWING

P.W. ASSEMBLY — DIGITAL INPUT UNIT

D | 09132 | 39842200

SCALE 2:1 | SHEET 1 OF 1

DWN	[illegible]	1-11-72	CONTROL DATA
CHKD	R. Gilbert	7-19-72	
ENG	R. Davidson	7-24-72	ANALOG - DIGITAL SYSTEMS DIVISION La Jolla, Calif. 92037
MFG	[illegible]		
APPR	E. [illegible]	7-26-72	CODE IDENT 09132
	A. Web	7-21-72	

TITLE: PW ASSY - DIGITAL INPUT UNIT

PREFIX	DOCUMENT NO.	REV
PL	39842200	F

FIRST USED ON

SHEET 1 OF 5

SHEET REVISION STATUS

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
A		RELEASED	B.J.	7-26-72	E.L.
B	13171	ADDED FN 33	TC	7-19-73	E.L.
C	13214	AUTOMATED P/L (WAS 3SN)	D.M.	2-1-74	E.L.
E	13298	DELETED F/N 32 (4 PLCS)	LVP	9-11-4	E.L.

NOTES:

DETACHED LISTS

AA3180

PRINTED IN U.S.A.

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER		PROCESSING DATE	PAGE NUMBER
39842200	F	CLA	A	PWA-DIG INPUT,LL (1NKT)	DS	1544-1	02/01/74		MF	04/08/75	~~1~~ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
10	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
13	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP5		N
11	B	15112700	200	PC	IC CKT 74L04	IN					PPP4		N
9	B	15112800	1800	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
20	C	24500036	1800	PC	RES FXD .25W 75 OHMS	IN					PPP5		N
18	C	24500055	200	PC	RES FXD .25W 750 OHMS	IN					PPP5		N
16	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP5		N
17	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP5		N
27	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
8	C	24505229	500	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN					PPP4		N
24	C	24562100	100	PC	TSTR SILICON-PLANAR,NPN	IN					PPP5		N
26	A	25175800	3600	PC	DIODE(1N914)	IN					PPP4		N
6	A	38958502	100	PC	TEST JACK, BLACK	IN					PPP4		N
5	A	38958507	200	PC	TEST JACK, YELLOW	IN					PPP4		N
7	A	38958509	100	PC	TEST JACK, PURPLE	IN					PPP4		N
25	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN					YYM4		N
28	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256				PPP4		N
12	B	39388300	100	PC	INT CKT 7400	IN					PPP4		N
14	B	39389200	200	PC	INT CKT (7440)	IN					PPP4		N
15	B	39389800	200	PC	INT CKT 74123	IN					PPP4		N
3	C	39827500	200	PC	GUIDE,APPROACH	IN					PPP4		N
1	C	39842100	100	PC	PWB-DIGITAL INPUT	IN					PPP4		N
34	C	39842300	REF	PC	LOGIC DIAGRAM (1NKT)	IN					FE4		N
29	A	39908200	300	PC	SCRE ,PAN HD,PHL-4-40 X1/4 IN	IN					PPP4		N
30	A	39908300	300	PC	NUT EM.PATTERN	IN					PPP4		N
31	A	39908400	300	PC	WASHER SPG LOCK	IN					PPP4		N
4	D	52036000	100	PC	AIR SEAL - 25 PAK	IN					PPP5		N
21	A	84996714	100	PC	CAP,CER 100V 120 PF	IN					PPP4		N
33	A	84996718	100	PC	CAP,CER 100V 270 PF	IN					PPP4		N
22	A	84996721	1800	PC	CAP,CER 100V 70 PF	IN					PPP4		N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N
					NUMBER OF LINE ITEMS = 31								
					HIGHEST FIND NUMBER = 34								

PROJECT ENGINEER
R.DENGLER

AA 2709 REV. 2-75

RECYCLE FOR THE FUTURE

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
39842201	F	C! A	A	PWA-DIG INPUT,LL (2NRT)	DS	1544-1	02/01/74	

MF

PROCESSING DATE	PAGE NUMBER
04/08/75	~~1~~ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
10	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
13	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP5		N
11	A	15112700	200	PC	INT CKT 74L04	IN					PPP4		N
9	A	15112801	1800	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
20	C	24500036	1800	PC	RES FXD .25W 75 OHMS	IN					PPP5		N
18	C	24500055	200	PC	RES FXD .25W 7[illegible] OHMS	IN					PPP5		N
16	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP5		N
17	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP5		N
27	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
3	C	24505229	500	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN					PPP4		N
24	C	24562100	100	PC	TSTR SILICON-PLANAR,NPN	IN					PPP5		N
26	A	25175800	3600	PC	DIODE(1N914)	IN					PPP4		N
6	A	38958502	100	PC	TEST JACK, BLACK	IN					PPP4		N
5	A	38958507	200	PC	TEST JACK, YELLOW	IN					PPP4		N
7	A	38958509	100	PC	TEST JACK, PURPLE	IN					PPP4		N
25	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN					SYM4		N
28	A	39181003	100	IN	INSULATION, TEFLON, 24 AWG	IN	013256				PPP4		N
12	B	39388300	100	PC	INT CKT 7400	IN					PPP4		N
14	B	39389200	200	PC	INT CKT 7440	IN					PPP4		N
15	B	39389800	200	PC	INT CKT 74123	IN					PPP4		N
3	C	39827500	200	PC	GUIDE.APPROACH	IN					PPP4		N
1	C	39842100	100	PC	PWB-DIGITAL INPUT	IN					PPP4		N
29	A	39908200	300	PC	SCREW,PAN HD,PHL-4-4 X1/4 IN	IN					PPP4		N
30	A	39908300	300	PC	NUT SM,PATTERN	IN					PPP4		N
31	A	39908400	300	PC	WASHER SPG LOCK	IN					PPP4		N
35	C	39915000	REF	PC	LOGIC DIAGRAM (2NRT)	IN					SFE4		N
4	D	52036000	100	PC	AIR SEAL - 25 PAK	IN					PPP5		N
21	A	84996714	100	PC	CAP,CER 100V 120 PF	IN					PPP4		N
33	A	84996718	100	PC	CAP,CER 100V 270 PF	IN					PPP4		N
22	A	84996721	1800	PC	CAP,CER 100V 70 PF	IN					PPP4		N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N

NUMBER OF LINE ITEMS = 31
HIGHEST FIND NUMBER = 35

PROJECT ENGINEER
R. DENGLER

AA 2709 REV. 2-73

RECYCLE FOR THE FUTURE

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
39842202	F	CLA	A	PWA-DIG INPUT,CC (2NST)	DS	1544-1	02/01/74	

MF

PROCESSING DATE	PAGE NUMBER
04/08/75	~~1~~ 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
10	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
13	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP5		N
11	B	15112700	200	PC	INT CKT 74L04	IN					PPP4		N
9	B	15112800	1800	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
20	C	24500036	1800	PC	RES F D .25W 75 OHMS	IN					PPP5		N
18	C	24500055	200	PC	RES FXD .25W 7[illegible] OHMS	IN					PPP5		N
16	C	24500063	100	PC	RES FXD .25W 1000 OHMS	IN					PPP5		N
17	C	24500094	400	PC	RES FXD .25W 20000 OHM	IN					PPP5		N
27	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
8	C	24505229	500	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN					PPP4		N
23	C	24505235	1[illegible]00	PC	CAP,FXD SOL TA 35V 3.3UF 1 PCT	IN					PPP4		N
24	C	24562100	100	PC	TSTR SILICON-PLANAR,NPN	IN					PPP5		N
26	A	25175800	3600	PC	DIODE(1N914)	IN					PPP4		N
6	A	38958502	100	PC	TEST JACK, BLACK	IN					PPP4		N
5	A	38958507	200	PC	TE T JACK, YELLOW	IN					PPP4		N
7	A	38958509	100	PC	TEST JACK, PURPLE	IN					PPP4		N
25	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN					AYM4		N
28	A	39181003	100	IN	INSULATION, T LON, 24 AWG	IN	013256				PPP4		N
12	B	39388300	100	PC	INT CKT 7400	IN					PPP4		N
14	B	39389200	200	PC	INT CKT (7440	IN					PPP4		N
15	B	39389800	200	PC	INT CKT 74123	IN					PPP4		N
3	C	39827500	200	PC	GUIDE.APPROAC	IN					PPP4		N
1	C	39842100	100	PC	PWB-DIGITAL INPUT	IN					PPP4		N
29	A	39908200	300	PC	SCRE[illegible],PAN HD,PHL-4-4(X1/4 IN	IN					PPP4		N
30	A	39908300	300	PC	NUT [illegible],PATTERN	IN					PPP4		N
31	A	39908400	300	PC	WASHER SPG LOCK	IN					PPP4		N
36	C	39915100	REF	PC	LOGIC DIAGRAM (2NST)	IN					FE4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP5		N
21	A	84996714	100	PC	CAP,CER 100V 120 PF	IN					PPP4		N
33	A	84996718	100	PC	CAP,CER 100V 270 PF	IN					PPP4		N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 OCKET	IN					PPP4		N

NUMBER OF LINE ITEMS = 31
HIGHEST FIND NUMBER = 36

PROJECT ENGINEER
R. DENGLER

AA 2709 REV. 2-73

RECYCLE FOR THE FUTURE

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER
39842203	F	C	A	PWA-DIG INPUT,CC (2NTT)	DS	1544-1	02/01/74	

MF

PROCESSING DATE	PAGE NUMBER
04/08/75	1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
10	A	15104200	500	PC	IC QUAD 2IN NAND GATE 7403	IN					PPP4		N
13	A	15104800	200	PC	IC SPEC DUAL D TYPE FF 7474	IN					PPP5		N
11	B	15112700	200	PC	INT CKT 74L04	IN					PPP4		N
9	B	15112800	1800	PC	MICRO CKT DTL HEX INVERTER	IN					PPP4		N
20	C	24500036	1800	PC	RES FXD .25W 75 OHMS	IN					PPP5		N
18	C	24500055	200	PC	RES FXD .25W 2? OHMS	IN					PPP5		N
16	C	24500063	100	PC	RES FXD .25W 000 OHMS	IN					PPP5		N
17	C	24500094	400	PC	RES FXD .25W 20000 OHMS	IN					PPP5		N
27	C	24501806	100	IN	WIRE ELECT SOLID COPPER 24 GA	IN					PPP1		N
8	C	24505229	500	PC	CAP,FXD SOL TA 35V 1.0UF 10PCT	IN					PPP4		N
23	C	24505235	1400	PC	CAP,FXD SOL TA 35V 3.3UF 1 PCT	IN					PPP4		N
24	C	24562100	100	PC	TSTR SILICON-PLANAR,NPN	IN					PPP5		N
26	A	25175800	600	PC	DIODE(1N914)	IN					PPP4		N
6	A	38958502	100	PC	TEST JACK, BLACK	IN					PPP4		N
5	A	38958507	200	PC	TEST JACK, YELLOW	IN					PPP4		N
7	A	38958509	100	PC	TEST JACK, PURPLE	IN					PPP4		N
25	B	38991203	100	PC	PATCHCORD 1 IN. LG.	IN					YYM4		N
28	A	39181003	100	IN	INSULATION. T FLON, 24 AWG	IN	13256				PPP4		N
12	B	39388300	100	PC	INT CKT 7400	IN					PPP4		N
14	B	39389200	200	PC	INT CKT (7440)	IN					PPP4		N
15	B	39389800	200	PC	INT CKT 74123	IN					PPP4		N
3	C	39827500	200	PC	GUIDE,APPROACH	IN					PPP4		N
1	C	39842100	100	PC	PWB-DIGITAL INPUT	IN					PPP4		N
29	A	39908200	300	PC	SCREW,PAN HD,PHL-4-4 X1/4 IN	IN					PPP4		N
30	A	39908300	300	PC	NUT SM,PATTERN	IN					PPP4		N
30	A	39908400	300	PC	WASHER SPG LOCK	IN					PPP4		N
37	C	39915200	REF	PC	LOGIC DIAGRAM 2NTT)	IN					PFE4		N
4	D	52936000	100	PC	AIR SEAL - 25 PAK	IN					PPP5		N
21	A	84996714	100	PC	CAP,CER 100V 120 PF	IN					PPP4		N
33	A	84996718	100	PC	CAP,CER 100V 270 PF	IN					PPP4		N
2	C	94243400	100	PC	CONNECTOR-CARD MTG 62 SOCKET	IN					PPP4		N

NUMBER OF LINE ITEMS = 31
HIGHEST FIND NUMBER = 37

PROJECT ENGINEER
R. DEINGLER

AA 2700 REV. 2-73

RECYCLE FOR THE FUTURE

COMMENT SHEET

MANUAL TITLE CONTROL DATA® DA101/DA401 Digital Input Unit Hardware

Maintenance Manual

PUBLICATION NO. 88980200 REVISION B

FROM NAME: _____

BUSINESS
ADDRESS: _____

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

FIRST CLASS
PERMIT NO. 333

LA JOLLA, CA.

BUSINESS REPLY MAIL

NO POSTAGE STAMP NECESSARY IF MAILED IN U.S.A.

POSTAGE WILL BE PAID BY

CONTROL DATA CORPORATION
PUBLICATIONS AND GRAPHICS DIVISION
4455 EASTGATE MALL
LA JOLLA, CALIFORNIA 92037

ATTN: PUBLICATIONS DEPARTMENT

FOLD

CUT ALONG LINE

STAPLE

STAPLE